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Observation of insulating and metallic-type behavior in Bi_2Se_3 transistor at room temperature

V. Gunasekaran, G. H. Park, K. S. Kim, M. Suemitsu, H. Fukidome*

Research Institute of Electrical Communication, Tohoku University, 2-1-1, Katahira, Aoba-ku, Sendai 980-8577, Japan

guna@riec.tohoku.ac.jp, *fukidome@riec.tohoku.ac.jp

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Topological insulators are a new class of electronic materials with promising device applications. In this work, multi-layer Bi_2Se_3 field effect transistors (FETs) are prepared by standard lithography followed by mechanical exfoliation method. Electrical characterization of the FET has been studied at room temperature. We observed both insulating and metallic-type transport behavior when device was gate-biased. Electron-phonon scattering plays a vital role in observing this behavior. We assume that this sort of behavior could be raised from the inherent metallic surface and semiconducting interior bulk properties of Bi_2Se_3.

Keywords: bismuth selenide, topological insulator, transistors.

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1. Introduction

Recently, topological insulators (Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3) have attracted much attention because of their bulk band gap (0.3 eV) and spin-polarized surface states with conductive massless Dirac Fermions [1]. Interestingly, Bi_2Se_3 has rhombohedral crystal structure which consists of Se or Bi lattices in stacked manner with the sequence of Se-Bi-Se-Bi-Se. This forms a sheet-like structure in which the adjacent quintuple layers (QL) are bonded by van der Waals forces [2]. According to recent reports, Bi_2Se_3 has been found to have potential application in field effect transistors (FET), thermoelectric materials, low-power spintronics and opto-electronics. Particularly, Bi_2Se_3 nanowire FET exhibits superior current-voltage characteristics with a large On/off current ratio, well saturated output current, zero cutoff current, and sharp turn-on voltage [2–5]. These unique properties open up a new consideration of Bi_2Se_3 as a potential candidate in spintronics and nanoelectronics.

There are few reports available on electrical transport studies of Bi_2Se_3 nanowire transistor [3], epitaxial growth of Bi_2Se_3 thin films [4], ultra-thin Bi_2Se_3 thin film [6], and few-layer nano-plates [7]. All these transport studies were investigated in low-temperature environment. When an ultra-thin (thickness $\sim$3.5 nm) sample with approximately 3 QL investigated, a strong insulating state was observed. However an improved conductance was observed for the samples with thicknesses of 6.5 nm to 14 nm [3].

Yet, up to now, much less attention has paid to investigations on room-temperature transport measurement of Bi_2Se_3 transistors. The reason behind that, since Bi_2Se_3 has gapless surface states, it could show surface metallic conduction however the bulk transport conduction cannot be easily identified at room temperature. As reported by H. Zhu et al, by tuning gate electric field at different temperatures, the bulk transport conduction can be isolated from the surface metallic conduction [3]. In this work, we fabricated multi-layer (ML) Bi_2Se_3 transistor (back-gated) and investigated their characteristics at room temperature. We observed both insulating and metallic-type transport behavior when the device was gate-biased.

2. Experimental

2.1. Sample preparation

High quality 2D n-Bi_2Se_3 crystals were purchased from 2D Semiconductors Co. Mechanical exfoliation method was used to remove the Bi_2Se_3 layers by peeling off, followed by transferring the layers into SiO_2/Si substrates (resistivity $\sim$ 1–15 ohm cm^{-1}). Heavily p-doped silicon with a 90 nm thick thermally grown SiO_2 top layer was used as substrates. Before transferring the layers, the substrates were well cleaned ultrasonically with acetone, ethanol and DI water. ML Bi_2Se_3 flakes were visually identified by using an optical microscope and chosen for device fabrication. Further confirmation for the number of layers in the sample was verified using Raman spectroscopy. We measured the thickness of Bi_2Se_3 layer as 143 nm using Bruker (Model: Dektak XT) thickness measurement system.

2.2. Device fabrication

We used a standard photolithography processes to make an electrode pattern. Mask aligner instrument (SUSS MicroTec; Model: MJB4, GmbH, Germany) was used. The photoresist (PR) AZ 5214E was spin-coated over the sample and UV light was exposed through Cr mask. Electron-beam evaporation [Sanyu Electron Model: SVC-700, LEB/4G] method was used to make Ti/Au (10/30 nm) electrodes as source and drain and structured by lift-off using acetone. Silver contact was made to Si substrate as back-gate. Detailed lithographic processes are schematically shown in Fig. 1. The channels of these fabricated Bi_2Se_3 transistor are 10 μm in length and 12 μm in width. After fabrication, the electrical transport characteristics of the devices were analyzed with semiconductor device analyzer (Agilent Technologies, Model: B1500A). These measurements were carried out under ambient conditions.

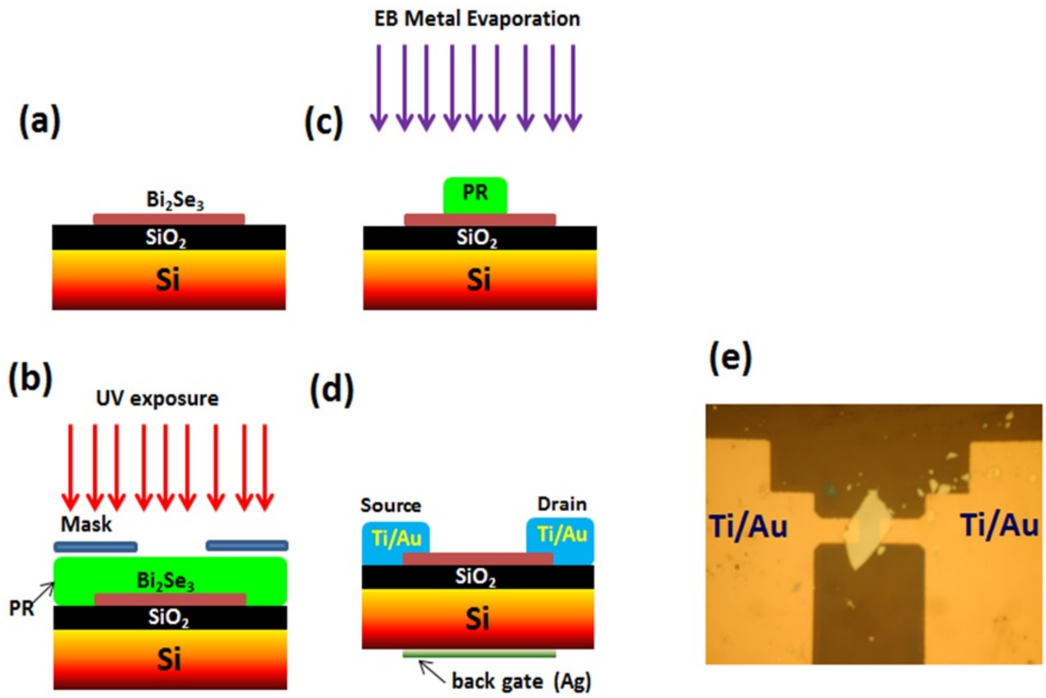

FIG. 1. (a) ML Bi_2Se_3 is transferred on SiO_2/Si substrate using mechanical exfoliation; (b) Photo-resist (PR) AZ 5214E is spincoated over the sample and UV exposure through Cr mask; (c) Evaporation of Ti/Au metals over the sample using electron beam evaporation method; (d) after lift-off process, the fabricated device with source, drain electrode pattern and back-gate (Ag electrode) configuration; (e) Optical image of fabricated FET device with Ti/Au electrodes

3. Results and discussion

Figure 2 shows the Raman spectrum of ML Bi_2Se_3 in the range of 100 – 250 cm^{-1}. Raman spectroscopy is mainly used to identify and confirm the number of layers present in the sample [8, 9].

We carried out Raman spectroscopy measurements using a micro-Raman spectroscopy system (model: Renishaw inVia) with a 514.5 nm laser excitation source. The power of incident laser was set as 35 mW and was focused through a 100× objective. Two characteristic peaks were observed at ∼132.5 cm^{-1} and ∼176 cm^{-1}, which correspond to an in-plane mode (E_g^2) and an out-of-plane mode (A_{1g}^2) of Rhombohedral Bi_2Se_3 lattice vibrations respectively [10–12]. According to Zhao et al, the Raman active out-of-plane mode (A_{1g}^2) signal is strongly reduced in bulk Bi_2Se_3 crystal rather than strong sharp peak appeared for few layer QLs [13]. In our case of ML Bi_2Se_3 (thickness ∼143 nm), a diminution in signal (A_{1g}^2) was observed as appeared in Ref. 13, which further confirms sample's multi-layer nature.

The n-Bi_2Se_3 field effect transistor (FET) characteristic measurements were conducted on a probe station. The drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) under different gate bias (V_G) has been

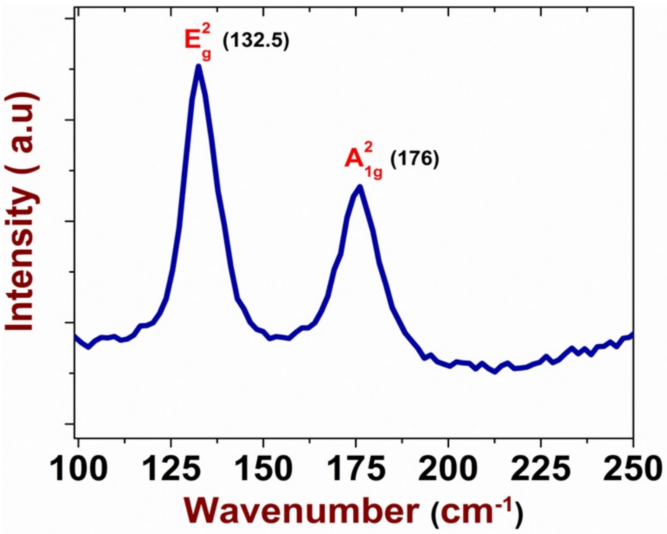

FIG. 2. Raman spectra of ML Bi_2Se_3 flake

measured at room temperature and the results are shown in Figure 3. The applied gate voltage is changed from −5 V to 5 V in 5 V steps. The output characteristics show an insulating and metallic-type behavior when the gate biases (V_G) is varied. At low gate-voltage ($V_G < 0$), no remarkable increase in drain current was observed. While increasing gate-voltage, a significant increase in drain current was observed. A sharp increase in drain current can be seen at $V_G = 5$ V in Fig. 3. By tuning the gate voltage, a metallic-like behavior was observed [14].

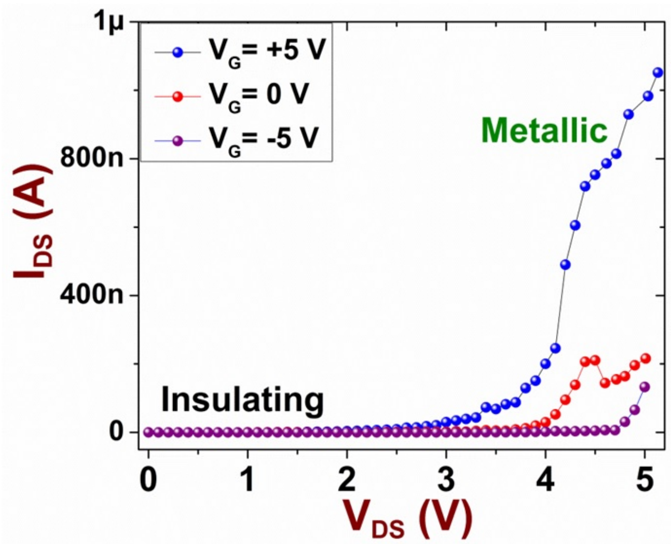

FIG. 3. I_{DS}-V_{DS} under different gate bias at room temperature

According to previous reports on Bi_2Se_3 nano-wire FET, a metallic-like conduction was observed where mobility-temperature relationship plays a mojor role in minimizing electron-phonon scattering at low-temperature (77 K) [15,16]. However, in our case, we observed both insulating and metallic-like transport behavior under different gate bias at room-temperature. At low-gate voltage ($V_G < 0$), the electron-phonon scattering is a dominating factor which limits the electron conduction causing insulating behavior in Bi_2Se_3 channel [16]. However, when gate bias is increased, the induced electron conduction dominates which suppress the electron-phonon scattering resulting metallic-like characteristics. We believe that the evolution of this metallic-type behavior at room temperature is attributed due to strong suppression of surface phonon scattering which has been achieved through gate-tuning.

Our results are further evidenced by previous observations where a strong insulating state was found in ultra-thin Bi_2Se_3 crystals (3 QL thickness $\sim$ 3.5 nm). But when the thickness of film is $\sim 6 - 14$ nm, a weakly insulating state was observed in Bi_2Se_3 thin films which is attributed mainly due to strong interlayer (top and bottom) couplings [3, 17–19]. This results in the absence of scattering which shows an increased contribution for the multi-layer ($>$ 100 nm) to the total carrier conduction. The amplitude of scattering and their related character as a function of thickness are associated with the topologically protected gapless surface states of Bi_2Se_3. Hence the electronic transport in ML Bi_2Se_3 is governed by both parallel surface and bulk contributions.

4. Conclusion

In conclusion, we have successfully fabricated ML n-Bi_2Se_3 FET and investigated their transistor characteristics at room temperature. Observation of both insulating and metallic transport in output characteristics further confirm that the intrinsic bulk bandgap nature and conductive surface states exist in Bi_2Se_3. Our findings may provide important guidance for the room-temperature transport studies on topological insulators.

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