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A QUANTITATIVE MODEL FOR QUANTUM TRANSPORT IN NANO-TRANSISTORS

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In a number of recent publications, a one-dimensional effective model for quantum transport in a nano-transistor was developed yielding qualitative agreement with the trace of an experimental transistor. To make possible a quantitative comparison, we introduce three phenomenological parameters in our model, the first one describing the overlap between the wave functions in the contacts and in the transistor channel, the second one is the transistor temperature, and the third one is the maximum height of the source-drain barrier. These parameters are adjusted to the traces of three experimental transistors. An accurate fit is obtained if the three adjustable parameters are determined for each gate voltage resulting in three calibration functions. In the threshold- and subthreshold regime the calibration functions are physically interpretable and allow one to extract key data from the transistors, such as their working temperature, their body factor, a linear combination of the flat band voltage and the built-in potential between substrate and source contact, and the quality of the wave function coupling between the contacts and the electron channel.

Keywords: nano-transistor, quantum transport, quantitative transistor model, nano-FET, drain current.

1. Introduction

The continuing reduction of the channel length for state-of-the-art nano-transistors necessitates a quantum mechanical treatment of carrier transport [1–3]. Here the solution of the Schrödinger equation can be achieved using a variety of methods. We choose the R-matrix formalism [4–13] to calculate the drain current of a planar MOSFET. In this approach it is possible to reduce in a systematic way a complete three-dimensional quantum-description of transport [6] to a one-dimensional effective model [7, 10, 11]. In this reduction process the assumption is made that only the lowest transverse mode in the electron channel contributes significantly to transport (single mode approximation, SMA). In Ref. [11], the SMA was shown to provide an accurate qualitative description of the drain current of an experimental nano-transistor. In this paper, our approach is extended to allow for a quantitative comparison with three further nano-transistors. To move from a qualitative to a quantitative description three suitable calibration parameters are introduced, one for the wave function overlap between the channel and the contacts, a second for the device temperature, and a third for the height of the source-drain barrier (calibrated SMA, cSMA). It is found that the cSMA allows an accurate fit for the $I_D - V_D$-traces of the experimental transistors if the three described parameters are determined for each gate voltage, resulting in three calibration functions. Even though the cSMA is a strongly simplified transistor model, a major advantage is that in the entire threshold- and subthreshold regime, all three calibration functions can be constructed in a simple and

physically interpretable way from four constants only (see dotted lines in Figs. 2 and 3). From the four fixed values of these constants, key data for the transistors can be extracted which take reasonable values.

2. Calibration of a one-dimensional effective transistor model

In the cSMA the drain current per width J is calculated according to:

$$J = CJ_0 \int_0^\infty d\epsilon \, [s(\epsilon - m) - s(\epsilon - m + v_D)] \, T(\epsilon). \tag{1}$$

In addition to the multiplicative parameter C for the wave function overlap between electron channel and contacts, Eq. (1) is equivalent to the corresponding expression in the SMA [10, 11]: The normalization constant for the current per width is given by $J_0 = 2eN_v^{ch}E_F/(h\lambda)$ where N_v^{ch} is the number of equivalent conduction band minima in the electron channel, E_F is the Fermi energy in the source contact, $\lambda = \hbar/\sqrt{2m^*E_F}$ is the scaling length, and m^* is the effective electron mass. The current transmission T in Eq. (1) is calculated from the right-moving scattering solutions of the normalized Schrödinger equation

$$\left[-\frac{1}{l^2}\frac{d^2}{dx^2} + v_{eff}(x) - \epsilon\right] \psi(x) = 0 \tag{2}$$

which is the one-dimensional effective Schrödinger equation (3) in Ref. [10] with energies normalized to E_F and lengths normalized to the channel length $L = l\lambda$ of the transistor. The normalized effective scattering potential is given by

$$v_{eff}(x) = \begin{cases} 0 & \text{for } x < 0 \\ v_0 - v_D x & \text{for } 0 \le x \le 1 \\ -v_D & \text{for } x \ge 1, \end{cases} \tag{3}$$

where $V_D = v_D E_F$ is the applied drain voltage and $V_0 = v_0 E_F$ is the maximum height of the source-drain barrier. (s. Fig. 1).

The effective potential is a Fowler-Nordheim-type field emission barrier used in the gate tunneling problem as well [15]. In the context of the transistor problem the simple trapezoidal form of the scattering potential corresponds to the neglect of image charges in the source-drain barrier associated with drain induced barrier lowering. In the effective potential v_{eff} the right-moving scattering states take the form $\psi(x < 0) = e^{ik_1 x} + re^{-ik_1 x}$ in the source and $\psi(x > 1) = te^{ik_2 x}$ in the drain, with $k_1 = \sqrt{l^2\epsilon}$ and $k_2 = \sqrt{l^2(\epsilon + v_D)}$. The transmission coefficient t is calculated solving the discretized Eq. (2) by a recursive procedure and the current transmission is then given by $T = k_1^{-1}|t|^2 k_2$. The first factor of the integrand in (1) is the difference of the supply functions in the source- and in the drain contact calculated from

$$s(\alpha) = \sqrt{\frac{u}{4\pi}} F_{-\frac{1}{2}}\left(-\frac{\alpha}{u}\right), \tag{4}$$

where F_j is the Fermi-Dirac integral of order $j = -1/2$ and $u = k_B T/E_F$ is the normalized temperature. The normalized chemical potential in the source contact is given by $m = \mu/E_F = uX_{\frac{1}{2}}[4/(3\sqrt{\pi}u^{3/2})]$, where $X_{1/2}$ is the inverse function of $F_{1/2}$. From Refs. [10] and [11] we adopt parameter values which are reasonable for a wide Si n-channel nano-FET with heavily doped contacts, $\lambda = 1$ nm, $J_0 = 5 \times 10^{-2} A/\mu m$, and $E_F = 0.35eV$.

Then, the channel lengths L =22 nm, 26 nm, and 30 nm of the three experimental transistors presented in the next section correspond to characteristic lengths of l =22, 26, and 30 and the chosen Fermi energy leads to $u \sim 0.1$ at room temperature.

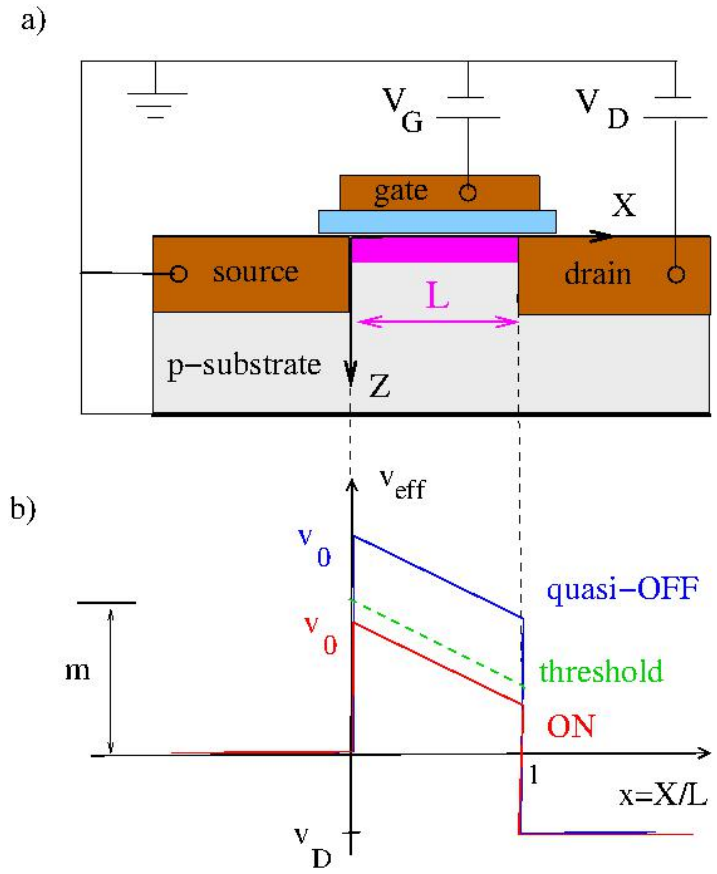

FIG. 1. a) Field effect transistor (here conventional n-FET) with external circuitry. b) Normalized effective potential v_{eff} in Eq. (3) at different applied gate voltages. Solid lines: Quasi-OFF-state, $v_0 > m$, corresponding to $I_D - V_D$ traces with positive curvature (s. filled rectangles in Fig. 2). Dashed lines: Threshold, $v_0 \sim m$, the $I_D - V_D$ trace exhibits a close-to-linear dependence on the drain voltage (s. asterisks in Fig. 2). Dotted line: ON-state corresponding to $I_D - V_D$ traces with negative curvature (s. open circles in Fig. 2). Shown here is the effective potential for gate voltages slightly above threshold. For larger gate voltages, v_0 increases above m because of device-heating (s. Fig. 3 (b)).

In the described one-dimensional effective model, neither the temperature, the barrier height nor the overlap parameter are known. To overcome this problem three calibration functions $u(V_G)$, $v_0(V_G)$, and $C(V_G)$ are introduced. These result from the minimization of the root mean square deviation

$$\Delta J_{rms}(V_G) = \sqrt{\frac{1}{N}\sum_i^N \left[\frac{J^{exp}(V_D^i, V_G) - J^{cal}(V_D^i, V_G)}{J^{exp}(V_D^i, V_G)}\right]^2} \tag{5}$$

at given V_G. Here $J^{exp}(V_D^i, V_G)$ is the experimental current measured at N equidistant drain voltages V_D^i where the calibrated theoretical current is calculated from (1) as

$$J^{cal}(V_D^i, V_G) = J(v_D = V_D^i/E_F, v_0, u, C, l = L/\lambda). \tag{6}$$

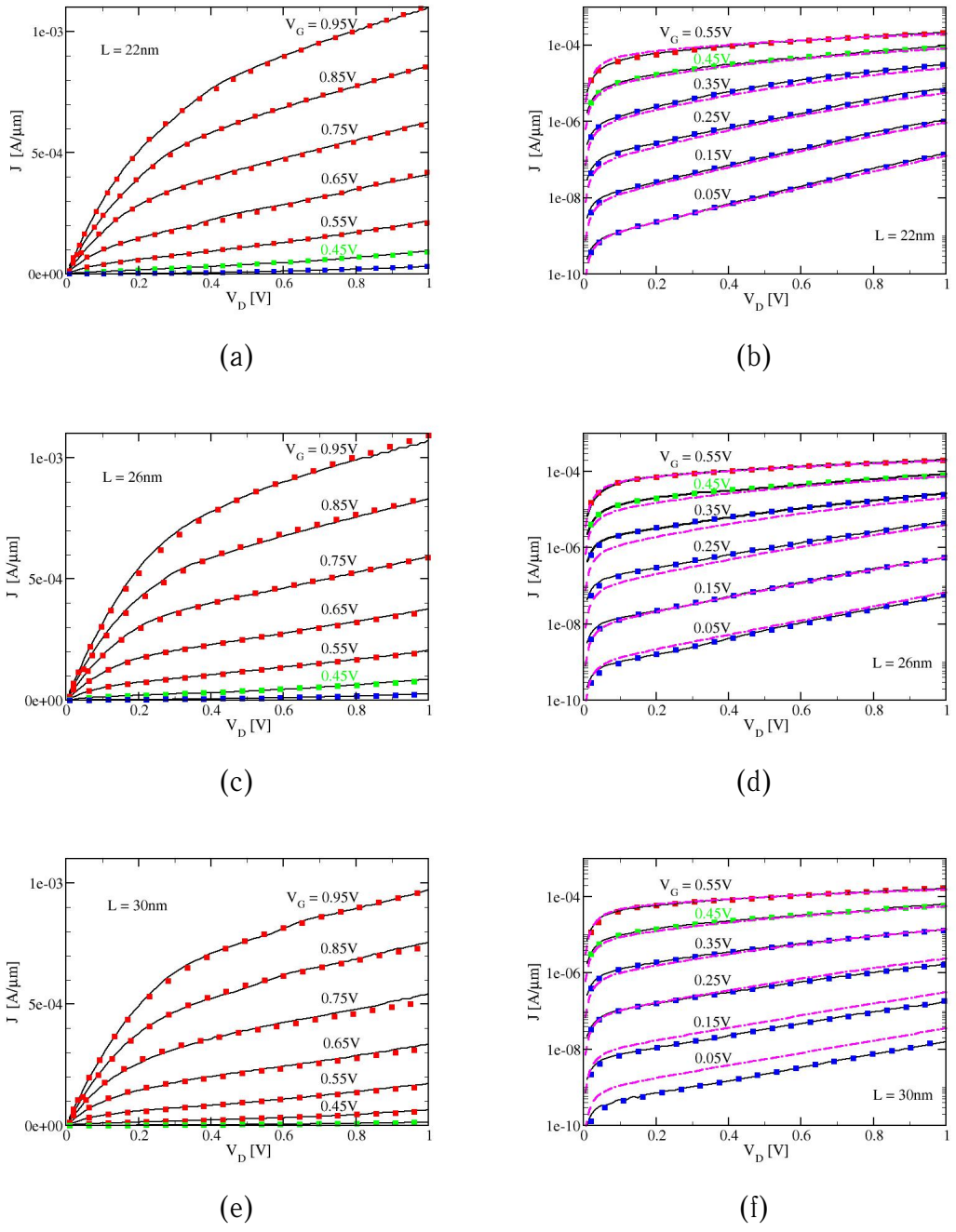

FIG. 2. In solid lines drain-characteristics J^{exp} of a series of n-channel nano-FETs with gate lengths of 22 nm ((A) linear scale and (B) logarithmic), 26 nm ((C) linear and (D) logarithmic), and 30 nm ((E) linear and (F) logarithmic). Marked with symbols J^{cal} according to Eq. (6): ON-state (open circles), experimental trace closest to the threshold trace at V_T (asteriks), and quasi-OFF-state (solid rectangles). In (B), (D), and (F) the dotted lines represent the four-constants-fit $u = 0.09$, $C = 0.1$, $\beta = 2/V$, $v_s^0 = -1V$ corresponding to the dotted lines in Fig. 3.

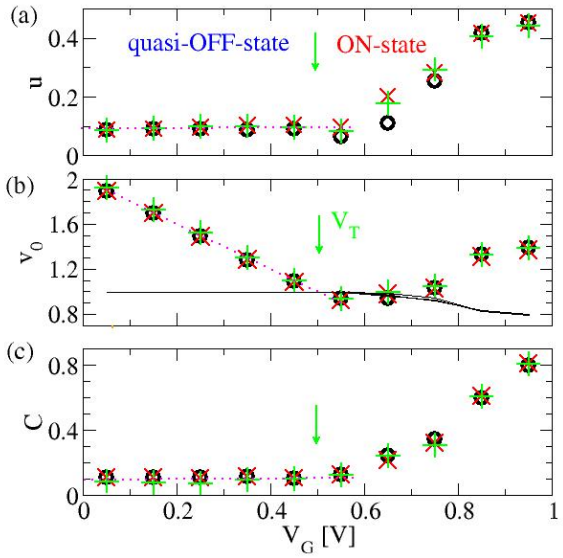

FIG. 3. Calibration functions (a) $u(V_G)$, (b) $v_0(V_G)$, and (c) $C(V_G)$, filled circles $L = 22$ nm, symbols $'x'$ $L = 26$ nm, and open rectangles $L = 30$ nm. In dotted lines the four-constants-fit $u = 0.09$, $C = 0.1$, $\beta = 2/V$, and $v_s^0 = -1V$. The solid black line in (b) marks the position of m.

The function $\Delta J_{rms}(V_G)$ is then minimized by varying in (6) the parameters C, v_0, and u. The parameter values leading to the minimum of $\Delta J_{rms}(V_G)$ constitute the calibration functions $u(V_G)$, $v_0(V_G)$, and $C(V_G)$.

3. Results

The drain characteristics, J^{exp}, of a series of three nano-FETs with different channel lengths but otherwise equal nominal device structure are shown in Fig. 2. These traces are compared to the calibrated theoretical current per width J^{cal} (s. Eq. (6)), demonstrating a good agreement between theory and experiment. The calibration functions $v_0(V_G)$, $u(V_G)$, and $C(V_G)$ obtained from the minimization procedure associated with Eq. (5) are plotted in Fig. 3. It can be determined that the calibration functions depend very little on the channel length. Furthermore, their gate-voltage-dependence shows two distinct regions separated by the threshold voltage $V_T \sim 0.5V$ (arrows in Fig. 3). Here, V_T follows from an inspection of the $I_D - V_D$-traces [11]: For gate voltages above V_T, in the ON-state, the traces show a negative curvature, while below V_T, it is positive. At $V_G = V_T$ there is a close-to-linear threshold $I_D - V_D$-trace (s. asterisks in Fig. 2).

We begin our detailed discussion of the calibration functions considering gate voltages below threshold: For $V_G < V_T$ the barrier height parameter decreases linearly with the gate voltage,

$$v_0(V_G) = -\beta V_G + v_0^0, \tag{7}$$

with $\beta = 2/V$ and $v_0^0 = 2$. To explain the linear relation in (7) we establish in the appendix the relation between the cSMA and the standard MIS capacitor model described in Refs. [16, 17]. As a result, within the depletion approximation to the standard MIS capacitor model the linear dependence can be attributed to a constant body factor n of the

transistor which is defined in Eq. (12). It can be calculated from β according to

$$n = \frac{q}{E_F \beta}, \tag{8}$$

yielding the value $n = 1.4$ for our transistors. This result lies within the typical values for bulk MOSFETs ranging between 1.2 and 1.5 [14] and it is close to $n = 1.6$ found from the measured subthreshold slope (s. Fig. 5). Furthermore, one obtains from the standard MIS capacitor model the following:

$$V_{bi} + \frac{1}{n} V_{FB} = \frac{E_F}{q} v_0^0, \tag{9}$$

i. e. v_0^0 represents the material constants V_{bi} and V_{FB} where V_{bi} is the built-in potential between the n^+-doped source contact and the p-substrate and V_{FB} is the flat-band voltage of the MIS-structure [16].

From Fig. 3 (c) it can be taken that in the threshold- and subthreshold regime the overlap parameter takes the constant value of $C = 0.1$. In the appendix we argue that within the depletion approximation to the standard MIS capacitor model, the transverse confinement potential in the electron channel is given by the acceptor density in the substrate, essentially independent of the gate voltage (s. Eq. (15)). Since the confinement potentials in source- and drain contact are essentially independent of the gate voltage as well, the transversal overlap of the wave functions is seen to be approximately constant. One can show that within SMA it holds that $0 \leq C \leq 1$, so that $C = 0.1$ indicates a rather poor wave-function-coupling between contacts and transistor channels caused by back-reflections.

Finally, in the threshold- and subthreshold regime the temperature calibration function in Fig. 3 (a) stays close to the room temperature value of $u \sim 0.1$. This is in agreement with the presence of only small tunneling drain currents in this regime leading to negligible Joule heating. To summarize, the results in Figs. 2 and 3 demonstrate that in the threshold- and subthreshold regime all $I_D - V_D$ traces of the three transistors can be derived from only four constants, namely $u = 0.09$, $C = 0.1$, $\beta = 2/V$, and $v_0^0 = 2$ ('four-constants-fit' in Figs. 2 and 3).

Above threshold voltage the chemical potential in the source contact rises above the maximum height of the barrier. Then the occupation of the lowest transverse level in the channel but also that of the higher transverse levels is strongly enhanced. This population of the electron channel leads to its widening as signaled by the increase in C. Furthermore, since the current grows due to the onset of classically allowed transport enhanced Joule heating occurs and the temperature increases rapidly. The widening of the electron channel and the heating of the transistor, in turn, favor the occupation of higher transverse channels in the electron channel and the SMA becomes invalid. As a consequence, the calibration parameters of the cSMA in Fig. 3 have to be regarded as pure fit-parameters in the ON-state. Therefore, at higher V_G one has to consider as an artifact, first, the extent of the transistor heating and, second, the extent of the reentrant increase for the maximum barrier height above the chemical potential.

4. Conclusions

The combination of the recently developed SMA and a special fitting procedure with three calibration functions yields excellent quantitative agreement with experimental data. In the threshold regime and below, the calibration functions can be calculated from four constants only. Making contact to the standard MIS-model, these four constants

can be physically interpreted, allowing one calibration function to extract central device parameters: The body factor, the built-in potential between source and substrate, the flat band voltage and the wave function overlap factor between electron channel and contacts.

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APPENDIX

A. Calibration functions in the standard MIS-model

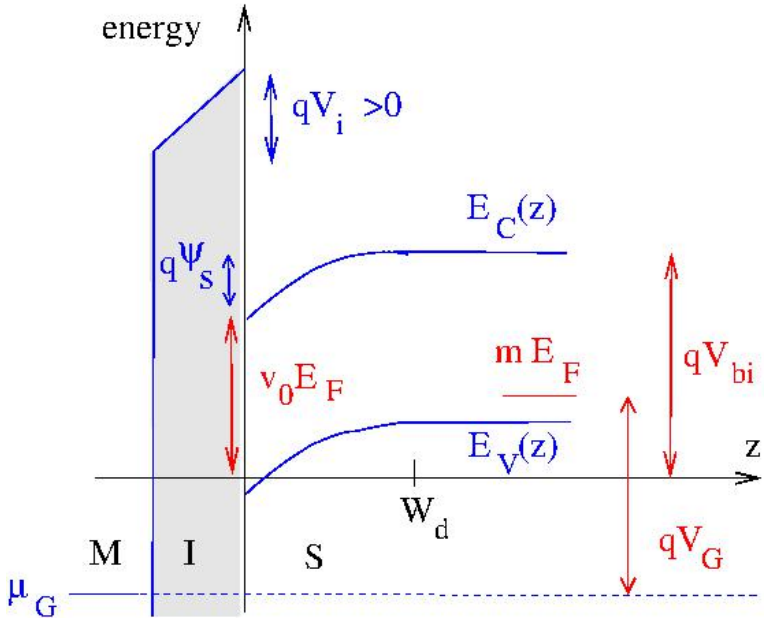

FIG. 4. Energy bands $E_{C/V}(z)$ of a standard MIS-structure (s. Fig. [2.35] in [16]) and energy levels in the cSMA (times-italic font and filled left right arrows, s. Fig. 1) in one diagram. To arrive at the basic relation Eq. (10), first, $E_C(0)$ is set equal to the height of the potential barrier, $v_0 E_F$ in Eq. (3). Second, one identifies $E_C(W_d) = qV_{bi}$ where W_d is the depletion layer width and qV_{bi} is the built-in potential between source contact and p-substrate.

In the threshold- and subthreshold regime, it can be assumed that the quantum mechanical electron charge in the transistor channel is negligible against the charge of the ionized acceptors, which can be treated in standard device theory (s. Sect. 2 of [16]). In this depletion approximation the position of the bottom of the conduction band $E_C(z)$ in the standard MIS-model can be associated with the transverse quantum-confinement potential $V(z)$ in the electron channel at zero drain voltage (s. Eq. (15)). For interpretation of the calibration functions in the cSMA we now plot in one diagram, shown in Fig. 4, the energy bands in the standard MIS-model (s. Fig. [2.35] in [16]) and the energy levels in the cSMA (filled left right arrows in Fig. 1). To construct a plot of these quantities in the common energy diagram the energy zero is set to the bottom of the conduction band in the source. Furthermore, we equate the chemical potential in the source contact, $\mu = mE_F$, with the chemical potential in the bulk of the p-substrate because, both, the source contact and the back gate are grounded. It is assumed that the host material in the substrate and in the grounded source are the same. Then, the bottom of the conduction band in the bulk p-substrate $E_C(z > W_d)$ is given by the built-in potential qV_{bi} between the isolated host materials of the source contact and in the substrate. The barrier height v_0 in Eq. (3) gives the position of the bottom of the conduction band $E_C(0)$ at the interface so that

$$v_0 E_F = E_C(0) = E_C(z > W_d) - q\Psi_s = qV_{bi} - q\Psi_s, \tag{10}$$

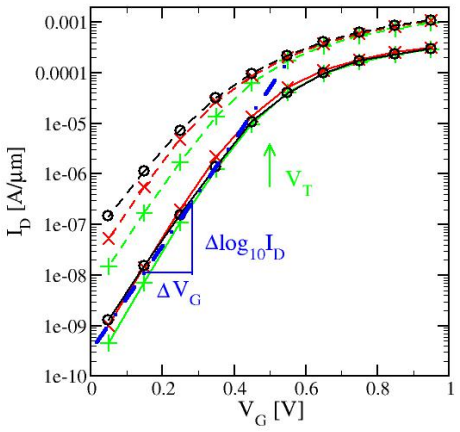

FIG. 5. Transfer characteristics of the experimental transistors in Fig. 3, dash-dotted lines for $V_D = 0.1V$ and dashed lines for $V_D = 1.0V$. Open circles $L = 22$ nm, filled triangles $L = 26$ nm, and symbols $'+'$ $L = 30$ nm. At the lower drain voltage, thermally activated behavior according to Eq. (14) is found with a slope $[d\log_{10} I_D/dV_G]^{-1} \sim 96mV/\text{decade}$, corresponding to $n = 1.6$ taken from the solid line. At the higher drain voltage thermal activation is overlayed with source-drain tunneling [11].

where Ψ_s is the potential drop across the space charge region of thickness W_d. Assuming a gate voltage controlled electron channel, one now writes in the standard MIS model the following:

$$V_G - V_{FB} = V_i + \Psi_s = -\frac{Q_s}{C_i} + \Psi_s, \tag{11}$$

where V_G is the applied gate voltage, V_i is the voltage that drops across the insulator barrier, $Q_s < 0$ is the total charge per area in the space charge region, and C_i is the constant insulator capacitance. In the depletion approximation the depletion layer capacitance can be written as $C_D = -\partial Q_s/\partial\Psi_s = \epsilon_s/W_d \sim \epsilon_s/W_{dm}$ [s. Eq. (2.201) of [16]]. Here, ϵ_s is the dielectric constant of the p-substrate, and around the threshold, we may replace W_d by its maximum value W_{dm} so that C_D is a constant. In this approximation Eq. (11) becomes $\Psi_s = (V_G - V_{FB})/n$ with a constant body factor

$$n = 1 + \frac{C_D}{C_i}. \tag{12}$$

Insertion of this result in the basic relation (10) leads to the following:

$$v_0 = \underbrace{-\frac{q}{nE_F}}_{\beta} V_G + \underbrace{\frac{q}{E_F}\left(V_{bi} + \frac{1}{n}V_{FB}\right)}_{v_0^0}. \tag{13}$$

This equation has the same form as the numerical quantum-result (7). A comparison of (13) and (7) yields Eqs. (8) and (9).

In the assumed approximation $W_d \sim W_{dm}$ one obtains from the standard model a constant inverse subthreshold slope [s. Eq. (3.41) in [16]]

$$S = \left[\frac{d\log_{10} I_D}{dV_G}\right]^{-1} = 2.3\frac{k_B T}{q} n, \tag{14}$$

which is found in the experimental transistors (s. Fig. 5) for small drain voltages. From the slope of the traces in their transfer characteristics one deduces $S = 96mV/\text{decade}$ and then from (14) it follows that $n = 1.6$.

To finally discuss the overlap calibration function, one interprets $E_C(z)$ as the transverse confinement potential $V(z)$ in the electron channel. In depletion approximation with $W_d \sim W_{dm}$ it follows that

$$V(z) \sim 2\Psi_B \left(1 - \frac{z}{W_{dm}}\right)^2 + qV_{bi} \tag{15}$$

[s. Eqs. (2.183) and (2.187) of Ref. [16]]. Here $\Psi_B = \mu_i - \mu$, where μ_i is the chemical potential of the intrinsic substrate semiconductor in the bulk. The channel confinement potential is seen to be essentially independent of the gate voltage. Therefore it is to be expected that the transversal overlap between the wave functions in the contacts and in the electron channel (and thus C) is independent of the gate voltage as well.