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Original article

How to make opposite state store again

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ABSTRACT The article shows the possibility of increasing the storage time of the opposite state (OS) at a temperature of 145 °C from 140 to 500 minutes in ferroelectric capacitors based on $Hf_{0.5}Zr_{0.5}O_2$ (HZO) by shift of current integration endpoint to right. Consideration of transient processes between measurement pulses after 500 minutes capacitors baking at 145 °C can enhance the OS retention from 21 to 35 % of the pre-heating state. Opposite trend detected for the same sate (SS) (decrease from 56 to 35 %) and new same state (NSS) (decrease from 63 to 45 %). It is also shown that the presence of a voltage shift caused by an imprint in some cases may not lead to a loss of polarization due to the current flowing during the flat part of the trapezoidal voltage pulse.

KEYWORDS TiN/HZO/TiN, retention, imprint, ferroelectric

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1. Introduction

Ferroelectrics based on HfO_2 are perspective materials for non-volatile memory application due to high scalability and process compatibility with complementary metal oxide semiconductor (CMOS) technology, in contrast to conventional ferroelectric materials [1,2]. In the case of ferroelectrics-based random access memory (FeRAM), information is stored in the orientation of the polarization and can be read by unipolar voltage pulse [3] subsequent analysis of the received current response. Data retention is one of the key metrics of non-volatile memory. Reliability studies focusing on data retention of HfO_2-based devices report about critical role of imprint in retention degradation [4–11]. The imprint effect manifests itself as a shift of the hysteresis Polarization–Voltage (P–V) loop along the voltage axis. It occurs during thermal bake and is a major issue for FeRAM reliability as it reduces the memory window [12]. Also, in some cases, polarization loss can be observed follow a few seconds after removal of the external electric field and attributed to relaxation processes [5].

The retention of the memory window, in the case of a MFM (Metal–Ferroelectric–Metal) capacitor, can be estimated by calculating the charge in electrical circuit during the supply of voltage pulse sequences [4, 13]. Pulse sequences form states which can be evaluate before and after baking: same state (SS), opposite state (OS) [13] and, in some cases, new same state (NSS) [4, 10]. Usually, OS demonstrates higher degradation rate in contrast to SS and NSS which usually explained by imprint [4–11]. However, imprint also influences on SS and NSS [11] and in case of non-saturated loop SS and NSS degradation rate can be higher than for OS [4]. Therefore, the reason for the usually observed OS higher polarization loss is not fully understood, and further research is required to carefully investigate the imprint influence and methods employed in calculating polarization loss. In this work, for the first time, we evaluate influence of charge integration intervals duration used for SS, NSS and OS calculation in relaxation (25 °C) and retention loss (145 °C) processes for $Hf_{0.5}Zr_{0.5}O_2$ (HZO) based capacitors with TiN electrodes.

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2. Experiments

To create TiN/HZO(10 nm)/TiN capacitors, magnetron sputtered was used to deposit TiN for both electrodes, and atomic layer deposition was used to grow HZO as a ferroelectric layer. After rapid thermal annealing in Ar atmosphere of 600 °C and 30 s capacitors with 250 μm^2 square were formed. The electric characteristics of the MFM devices were measured by Agilent B1500 semiconductor parameter analyzer. During all electric measurements, a voltage bias was applied to the top electrode and the bottom electrode was grounded and used for current measurements each 10 ns.

To evaluate retention loss and polarization relaxation of the TiN/HZO/TiN capacitors, pulse sequences “Cap 1” and “Cap 2” used for same-state (SS+), new same-state (NSS+) and opposite-state (OS+) determination accordance with [4, 10]. Pulses schemes used for these tests are illustrated in Fig. 1. According to [4], the polarization of SS+ was calculated as the difference between the polarizations of pulses 2_1 and 1_1, NSS+ – 2_3 and 1_2, and OS+ – 1_4 and 2_4 (Fig. 1). It is assumed that pulses 2_1, 2_3, and 1_4 contain a ferroelectric response (Data “1”), while pulses 1_1, 1_2, and 2_4 do not have a ferroelectric response (Data “0”). Polarization of each Data “1” and Data “0” pulses was calculated as total pulse charge normalized per MFM capacitor area. The charge, in turn, is calculated by integrating the current response. The time point at which integration begins corresponds to the start of the rise of the positive voltage pulse. The final time point of integration is specified separately.

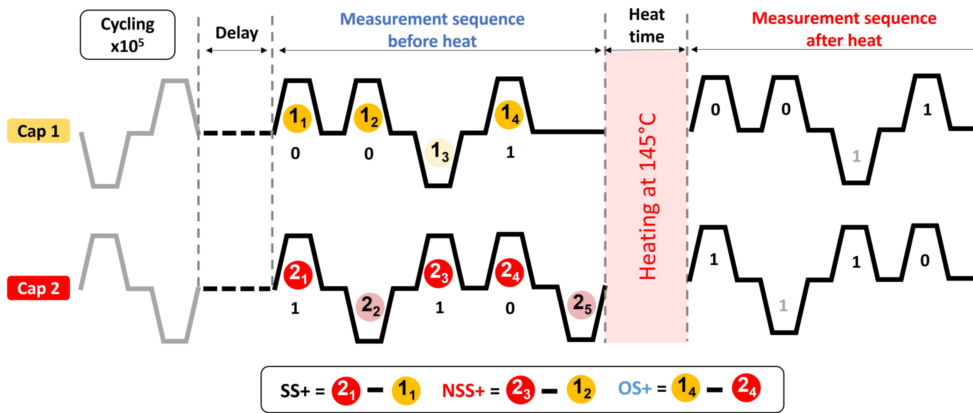

FIG. 1. Measurement sequences “Cap 1” and “Cap 2” used for relaxation and retention measurements

Before “Cap 1” and “Cap 2” sequences applying, were waked up by 10^5 cycles at room temperature (25 °C). For “Cap 1” and “Cap 2” sequences, last pulse of wake-up cycling was positive and negative, respectively. Than, to evaluate possible polarization relaxation before baking [5] “Cap 1” and “Cap 2” sequences were applied to capacitors with delay in the range from 1 μs to 100 s after wake-up cycling (Fig. 1). For retention measurements “Cap 1” and “Cap 2” sequences were applied to capacitors twice, first before baking (with delay of 1 μs after wake-up cycling at 25 °C) and second after 10, 40, 200 or 500 minutes of 145 °C baking according to [4]. At least 6 capacitors were used at each time point to calculate the polarization (3‘– for “Cap 1” and 3 for “Cap 2” sequences). 12 capacitors were used at 500 minutes of 145 °C baking time point (6 – for “Cap 1” and 6 for “Cap 2” sequences). Pulse amplitude and width for cycling and measurements sequences were equivalent and equal to 3 V and 3 μs respectively. Pulse shelf, rise and fall times were equal to 1 μs. Pulse separation was 1 μs. The pulse length and current measurement frequency were selected for more clear demonstration aspects of polarization calculation from current-time data for 250 μm^2 ferroelectric capacitors.

3. Results and discussion

Figure 2(a) shows evolution polarization values for all states in relaxation region at 25 °C and after baking at 145 °C. Charge integration range was 3.5 μs (pulse width and 500 ns after it) to take into account RC delay (Fig. S1(a), Supplementary materials). In relaxation region, polarization of SS+, NSS+ and OS+ after 1 μs delay is $\sim$30.2$\pm$0.8 $\mu C/cm^2$. After 100 s delay SS+, NSS+ and OS+ polarization demonstrate same values (negative states SS−, NSS− and OS− demonstrate similar trend in Fig. S2).

A noticeable drop in polarization is detected only after baking at elevated temperature. SS+, NSS+ and OS+ polarization after 10 minutes baking at 145 °C was 21, 22.5, and 18 $\mu C/cm^2$ respectively. Maximum degradation was achieved for 500 minutes baking at 145 °C, the values were 12.5, 15.5, and 9.5 $\mu C/cm^2$ for SS+, NSS+ and OS+ polarization, respectively. So, OS+ higher degradation is in accordance with previous research [5–8, 10, 14] and usually explained by shift of coercive fields (imprint), however, this effect also influences on SS and NSS [11]. Moreover, the imprint can start develop after 10^{-5} s [11], but in our case, polarizations values of all states do not change significantly even after 100 s. This raises two points that require clarification: the reason for the stronger effect of the imprint on OS compared to SS and NSS and the reason why the imprint does not result in a reduction in polarization during the relaxation process.

In order to do this, it is necessary to analyze the process of calculating polarization loss. First, it should be noted that usually reported only about polarization margin (Data “1” minus Data “0”) without separate analyzing of Data “1” and Data “0” [5–8, 14]. Second, time interval used for charge and polarization calculation measurement also usually is not specified. However, in real 1T-1C FeRAM devices, only after a certain time interval values Data “1” and Data “0” can be distinguished by the voltage difference on the bitline [9]. So, to recognize reasons of higher OS degradation, evolution of each pulse in “Cap 1” and “Cap 2” sequences and integration interval used for polarization calculation should be consider.

Figure 2(b) shows that in the relaxation region (25 °C) polarizations for all Data “0” and ”Data “1” values without any significant evolution are $\sim 0.4\pm0.4$ μC/cm^2 and $\sim30\pm0.4$ μC/cm^2, respectively. The observed error is related to the accuracy of the measuring source ($\sim$1.5 μA), and not to the presence of a leakage current, since the current at maximum voltage on the pulse shelf after an RC delay is comparable to the current without voltage supply (Fig. S1(b)).

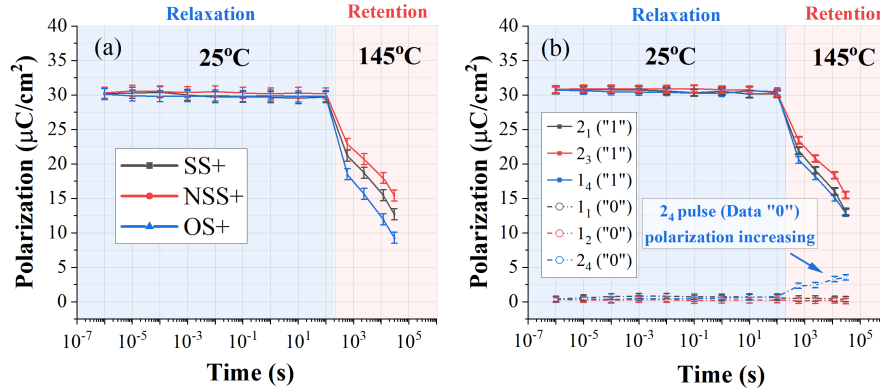

FIG. 2. Relaxation and Retention measurements of the TiN/HZO/TiN capacitors for (a) SS+, NSS+, OS+ and (b) pulses from “Cap 1” and “Cap 2” sequences. Charge measurement range was 3.5 μs (pulse width and 500 ns after it). The calculated values in each time point are in the ranges of $\pm$0.8 μC/cm^2 for (a) and $\pm$0.4 μC/cm^2 (b) and showed by error bars

Next, after 145 °C baking, Data “0” 2_4 pulse polarization demonstrate a noticeable increase – to 2.5 μC/cm^2 after 10 minutes, and 3.5 μC/cm^2 after 500 minutes baking. In contrast, other Data “0” pulses polarization (1_1 and 1_2 pulses) is not affected by baking. In turn, all ”Data “1” polarization values demonstrate degradation after baking. 2_1 (SS+), 2_3 (NSS+) and 1_4 (OS+) pulses polarizations after 10 minutes baking were 22, 23, and 20.5 μC/cm^2, respectively. Maximum degradation was achieved after heating for 500 minutes, the values were 13, 16, and 13 μC/cm^2 for SS+, NSS+ and OS+ polarization, respectively.

Thus, higher OS+ degradation in compare with SS+ during baking can be caused by polarization increasing of 2_4 pulse, because changes in 1_1 pulse (Data “0”) are insignificant and degradation ferroelectric 2_1 and 1_4 pulses is comparable. 2_3 pulse (NSS+) higher polarization value can be caused by recovery process after 2_1 and 2_2 pulses [14, 15]. It should be noted that effect of non-zero Data “0” current response detected on 2_4 pulse was reported previously and can be attributed to ferroelectric contribution [10].

Therefore, the analysis of current responses used in calculating the polarization can be useful in understanding the processes (imprint and ferroelectric contribution) taking place in the capacitor (Fig. 3). Changing dynamic of pulses responsible for SS+ and NSS+ are similar: first, there are no significant evolution in current responses of “Data 0” pulses (1_1 and 1_2), second, shifting maximum currents of “Data 1” pulses (2_1 and 2_3) to higher voltages during relaxation and retention measurements (Fig. 3(a–d)). After 100 s delay, maxima of ferroelectric current responses for 2_1 and 2_3 pulses shift to higher voltages on 0.5 and 0.3 V respectively in contrast to 1 μs delay (Fig. S3) and could be associated with imprint recovery for 2_3 pulse [14], however, this imprint does not lead to difference in polarization values (Fig. 2b).

Also, in both cases (2_1 and 2_3 pulses) increasing of backswitching effect detected during voltage fall after baking (Fig. 3(a,c)). For OS+ pulses (1_4 and 2_4) evolution processes show significantly different dynamic in contrast to SS+ and NSS+ pulses: shift current maxima of 1_4 pulse to lower voltages (Fig. 3(e)) and ferroelectric response detection in pulse 2_4 (Fig. 3(f)). In contrast to “Data 1” pulses for SS+ and NSS+ (2_1 and 2_3) there is no backswitching effect for “Data 1” pulses for OS+ (1_4 pulse) after baking. In turn, backswitching effect detected in “Data 0” pulse of OS+ (pulse 2_4). Also, it should be noted that for all pulses with backswitching effect (2_1, 2_3, 1_4) transient current after the pulse end is detected and may influence on polarization calculation [11].

To evaluate influence of transient currents on polarization calculation three time intervals were used: “I1” – 3 μs (only voltage pulse without RC-delay), “I2” – 3.5 μs (used in Fig. 2) and maximum “I3” – 4 μs (Fig. 4).

Increasing of time interval leads to a decrease of calculated polarization values for all pulses. In the relaxation region, calculated polarization for all Data “1” pulses decreases from $\sim$33 μC/cm^2 for “I1” to $\sim$31 μC/cm^2 for both “I2” and

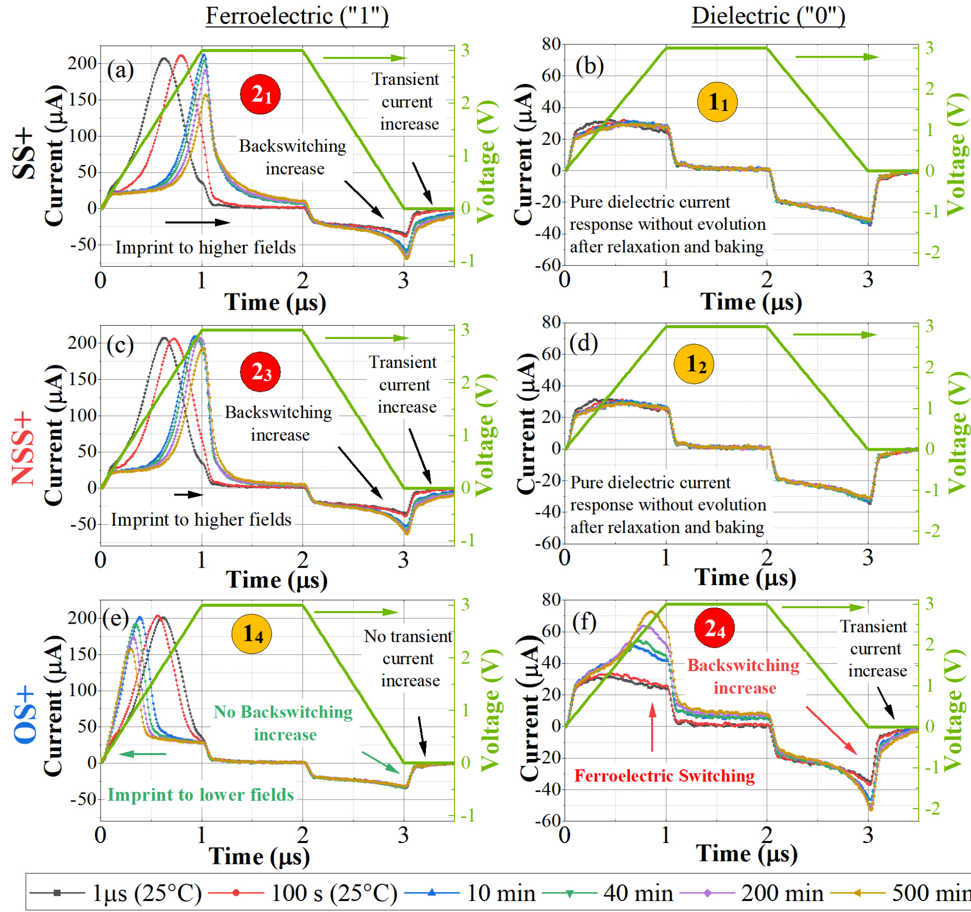

FIG. 3. Current responses of pulses from "Cap 1" and "Cap 2" sequences used for SS+ (a, b), NSS+ (c,d), OS+ (e,f) calculation

"I3". For all Data "0" pulses polarization decreases from ∼2 μC/cm^2 for "I1" to ∼0.8 μC/cm^2 for both "I2" and "I3" (Fig. 4 black and red curves). It is worth noting that Fig. 3(a) and Fig. 4(a) illustrate the reason for the lack of polarization loss during the observed imprint. In case of 1 μs delay most of the charge generated by the ferroelectric switching falls within the medium voltage rising range (∼ 1.9 V in Fig. S3, black curve). In contrast, for a delay of 100 seconds, the same charge flows at higher voltages (∼2.4 V Fig. S3, red curve) and on the flat part of the trapezoidal voltage pulse.

The changes in the integration interval are most pronounced when calculating the polarization after baking for pulses with backswitching (2_1, 2_3, 2_4) For pulse 2_1 after 500 min baking polarization decrease from 19 μC/cm^2 ("I1") to 12 μC/cm^2 ("I3") (Fig. 4a). For 2_4 pulse polarization decrease from 8 μC/cm^2 ("I1") to 2.8 μC/cm^2 ("I3") (Fig. 4d). Therefore, SS+ polarization value after 500 min baking is 17 μC/cm^2 in case of "I1" interval, 13 μC/cm^2 ("I2") and 11.5 μC/cm^2 ("I3"). OS+ polarization value after 500 min baking is 6 μC/cm^2 in case of "I1" interval, 9.5 μC/cm^2 ("I2") and 10.5 μC/cm^2 ("I3"). So, it shows practically equivalent polarization loss for SS+ and OS+ estimated by long pulse interval. The trend for NSS+ is similar to SS+ with effect of partial recovery (not shown).

Interval influence on normalized polarization loss after baking shows in Fig. 5 (SS+ and OS+) and Fig.S4 (NSS+). Maximum difference between states detected for I1 interval after 500 min backing: 56 %, 63 % and 21 % from initial polarization for SS+, NSS+ and OS+ respectively. An increase in the integration interval leads to reducing SS+, NSS+ and increasing OS+ values. The SS+ and OS+ normalized polarization values for I3 interval after 500 min backing practically the same and equal to ∼35 % from initial polarization. For NSS+ normalized polarization value for I3 interval is 45 % after 500 min backing.

It can be seen that an increase in the integration interval leads to an increase in OS+ storage time. At longer integration intervals, the levels of degradation of the SS+ and OS+ states become comparable (green lines in Fig. 5). The same level of normalized OS+ losses (35 % Fig. 5) for the short interval ("I1") it is achieved after ∼ 140 minutes of exposure at 145 ° C, and for the "I3" interval only in 500 minutes.

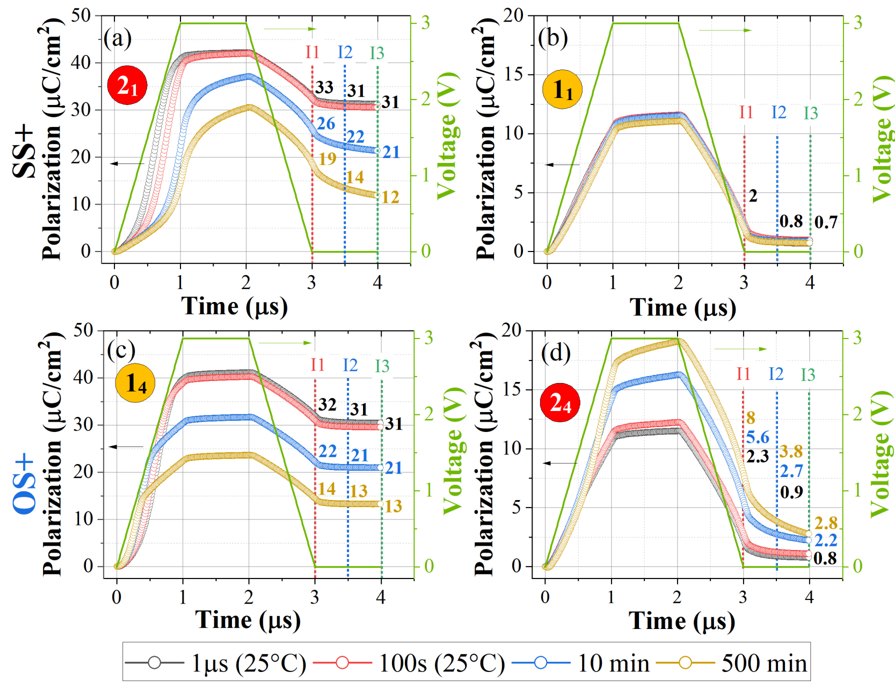

FIG. 4. Change of the polarization value depending on the integration interval for 2_1 (a), 1_1 (b), 1_4 (c) and 2_4 (d) pulses. Numbers indicate polarization values for “I1”, “I2” and “I3” intervals

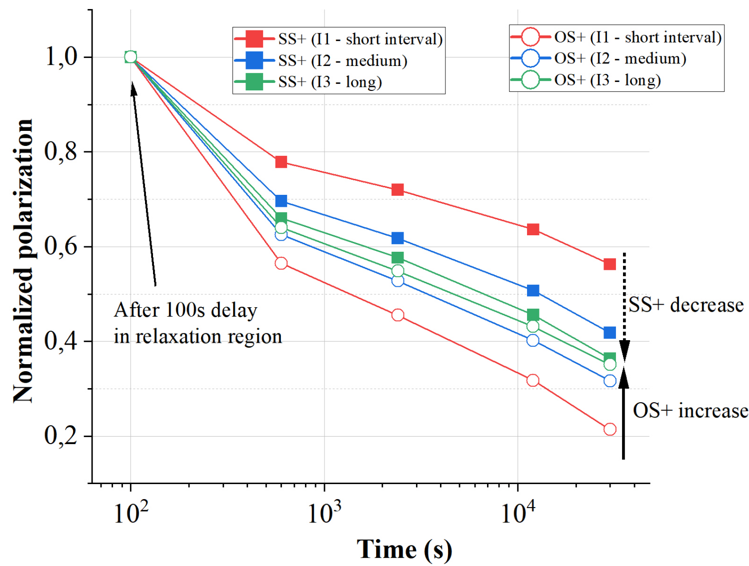

FIG. 5. Comparison of normalized polarization loss of SS+ (closed squares) and OS+ (open circles) for different integration intervals after baking at 145 °C

4. Conclusion

The results presented above show that the shift of the integration endpoint to longer times and the corresponding extension of the integration interval from 3 to 4 μs improve the OS+ retention time in ferroelectric TiN/HZO (10 nm)/TiN capacitors from ∼140 to 500 min at 145 °C. It is also shown that the coercive voltage shift, which is often cited as an unambiguous precursor to read polarization degradation, may not lead to polarization loss in the case of trapezoidal control pulses due to the charge flowing on the pulse shelf.

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