

## Impact of the channel shape, back oxide and gate oxide layers on self-heating in nanoscale JL FINFET

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**ABSTRACT** We study the impact of channel shape, back oxide, and gate oxide on the self-heating performance in nanoscale junctionless Fin Field Effect Transistor through numerical simulation. The role of back oxide and gate oxide layers in setting the channel temperature is compared. Simulation results show that in the case of hafnium oxide (HfO<sub>2</sub>) as the gate oxide and silicon dioxide (SiO<sub>2</sub>) as the back oxide, the main role in setting the channel temperature corresponds to the base width of the channel that is in contact with the back oxide layer.

**KEYWORDS** self-heating effect, junctionless FinFET, channel shape, channel temperature.

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### 1. Introduction

Over the last few decades, the capabilities of metal-oxide-semiconductor field effect transistor (MOSFET) characteristics have adapted to a variety of CMOS integrated circuit (IC) applications [1–4] and have led to various new requirements for MOSFET characteristics and parameters. One of these requirements is the increasing degree of the integration and the reduction in IC power consumption. This requirement is mainly related to the reduction in size of the transistors included in the IC as a component. MOSFET, especially junctionless (JL) MOSFET [5], is one of the widely used transistor ICs. Currently, most transistor structures are based on JL transistors such as bulk planar BPJLT, double gate JL transistors, multi-gate JL transistors, silicon on insulator (SOI) JL transistors, and gate all around JL transistors. When the MOSFET sizes are reduced, the various types of degradation effects, for example short channel effects and random telegraph noise, are increased [6, 7]. In order to reduce the short-channel effects, the triple-gate Fin Field Effect Transistor (FinFET) [8] and then the JL-FinFET [9] based on SOI technology were proposed. In these transistors, the back oxide is in contact with the channel and it has considerably low thermal conductivity relative to the silicon substrate, which is generally used in bulk MOSFETs. This leads to an accumulation of heating in the transistor channel (self-heating effect (SHE)) [10]. The SHE influences the drain current and changes the characteristics of the transistor. For the SHE in FinFETs, various methods and the structures of transistors able to reduce this effect were considered in many works [11–15]. In [11], the charge plasma (CP) based JL MOSFET on a selective buried oxide (SELBOX-CPJLT) is proposed. This approach is used to reduce the SHE presented in SOI-based devices. The proposed device shows better thermal efficiency compared to SELBOX-JLT, which has not charge plasma. The impact of the Gaussian channel doping profile (GCD) in enhancing the double gate (DG) JL MOSFET reliability against SHE is presented in [12]. It is found that the amended channel doping has a profound implication in improving both the device's electrical performance and the reliability against the undesired SHE. The role of the gate oxide layer in the SHE was considered in [13]. The SHE for a vacuum gate dielectric (VGD) tri-gate FinFET versus a high-k (HK) tri-gate dielectric FinFET were investigated. Simulation results show that the VGD device has fiercer SHEs than the HK device, resulting in greater saturation current degradation. This is due to the low thermal conductivity of the gas around the channel, which impedes the heat diffusion to the sinks and increases the peak temperature in the hot spot region. The influence of the material of the back oxide layer

on the SHE was considered in [14]. In this work, aluminum nitride is used as the back oxide in a Si MOSFET (SOAN MOSFET) and a strained Si/SiGe layer is formed on a SOAN substrate called SGSOAN nMOSFET. Further, the thermal properties of SGSOAN nMOSFET and SGOI nMOSFET with different channel expansions/dimensions are compared.

In Ref. [15], a device structure called an undoped buried region MOSFET (UBR-MOSFET) by introducing a region that acts as an undoped region under the channel and an oxide buried only under the source and drain regions was simulated to examine the current of drain and temperature distribution due to SHE. The higher thermal conductivity of the UBR region is shown to lead to more efficient heat dissipation.

Other interesting works have also considered the influence of channel shape on the performance of FinFET and JL FinFET [16–19]. In [16], it is shown that the transistor threshold voltage dependence on the channel doping concentration is different for different JL FinFET channel shapes. This is attributed to stronger gate coupling, since the gate plane is closer to the bottom of the channel with the non-vertical sidewalls of the triangular fin device compared to the rectangular fin device. The effect of fin shape on the thermal resistance of the proposed irregular SOI FinFET is analyzed in [17]. It is shown that the SHE can be controlled by regulating the corner effect by using the rounded shape of edges.

Overall, analysis of the literature related to SHE in FinFET and particularly in JL FinFET shows that the influence of the shape of the channel on SHE has not been taken into account, whereas in the nanoscale JL FinFETs, the variability of the shape of the channel can take place. To investigate this very important issue, which is not covered in the literature, this work uses a 3D simulation to compare the role of the gate oxide and back oxide layers in SHE in nanometer size JLFinFETs with different channel shapes.

This paper is organized as follows: Section 2 analyzes the different shapes of the JL FinFETs and provides a clear definition of the parameter settings that are used for the simulation. Section 3 focuses on both the presentation and discussion of the simulation results. Finally, in Section 4, important concluding remarks are formulated.

## 2. Device structure and simulation setup

In order to compare the influence of the back oxide and gate oxide layers on the SHE in nanoscale JL FinFETs, the devices with different channel shapes and constant cross-sectional areas are considered for the study. Two groups of junctionless FinFETs are considered for the study. In the first group, the transistors with a rectangular cross-section, different thickness  $T_{Si}$  and width, but with a constant cross-sectional area were considered, as shown in Fig. 1.

In the second group, the channel base width  $W_{Si}$  and cross-section area are constant, while the shape of the channel cross-section is changed from a rectangle to a trapezoid shape, as shown in Fig. 2. The ratio of channel thickness to the channel base width ( $T_{Si}/W_{Si}$ ) is used as a parameter that reflects the channel shape. The structures shown in Fig. 1 and Fig. 2 are designed and simulated using Sentaurus TCAD 3D device simulator [20]. Along with the default model, the models for mobility degradation were included in order to take into account the mobility dependency on the doping concentration.

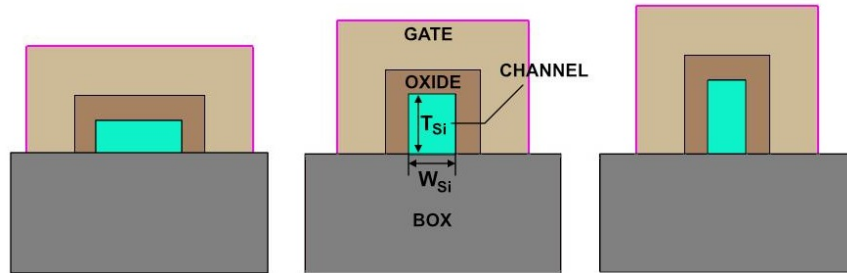


FIG. 1. Schematic of JL FinFETs with rectangle channel cross-section shape, the different ratio between width and thickness of the channel, and constant area of the cross-section

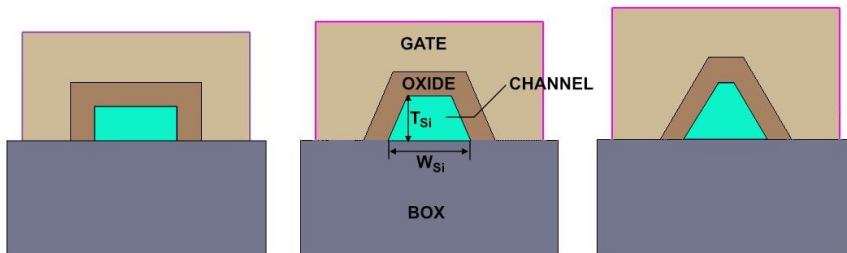


FIG. 2. Structures of simulated JL FinFETs with rectangle and trapezoid channel cross-section shape, constant area of the channel cross-section and base width, while the different thickness of the channel

For the simulation, scattering due to impurities and the effect of high fields to take into account the velocity saturation of charge carriers as well as the effect of the normal component of the field to take into account the effect of the interface on the drain current are considered. To account for the SHE, the thermodynamic transport model and the Shockley–Reed–Hall recombination model were used. Since we used a dielectric with high dielectric permittivity as the gate dielectric, the relevant mobility degradation model, the Lombardi model was used, which includes empirical degradation terms accounting for remote Coulomb scattering and remote phonon scattering. A quantum correction with regard to the density gradient is used in both drift-diffusion and thermodynamic models [21]. The device and the model used were calibrated based on the experimental results reported in [22]. The parameters considered for the simulation are shown in Table 1 and the transfer characteristics are depicted in Fig. 3. This device's parameters mainly correspond to the CMOS technology node of 10 nm.

TABLE 1. Parameters considered for Device Simulation

Parameters	Designation	Values
Si channel doping level	$N_{sub}$	$5 \cdot 10^{18} \text{ cm}^{-3}$ (n-type)
Thickness of $\text{HfO}_2$ gate oxide layer	$t_{ox}$	6.7 nm ( $t_{eqv} = 1.2$ nm)
Channel thickness	$T_{si}$	9–22 nm
Width of the channel base	$W_b$	22–5 nm
The thickness of the $\text{SiO}_2$ back oxide layer	$T_{box}$	145 nm
Width of the $\text{SiO}_2$ back oxide layer	$W_{box}$	69.4 nm
TiN Gate length	$L_{gate}$	10 nm

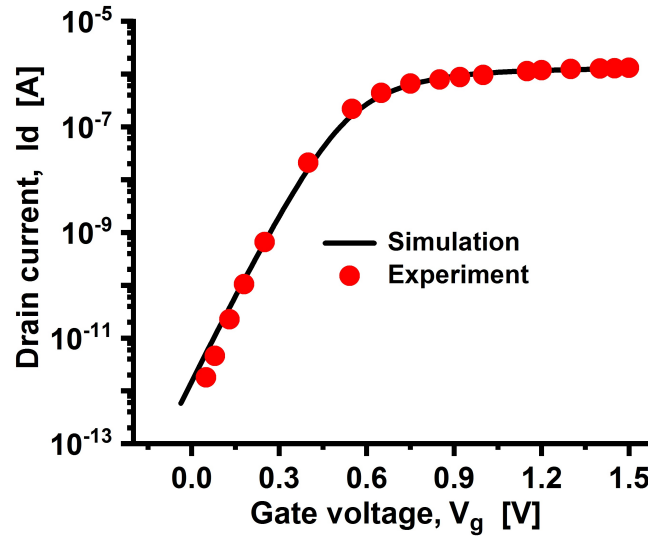


FIG. 3. Transfer characteristics of simulated and experimental transistors taken from [22], with the same geometries and parameters

### 3. Results and discussion

The main source of heat dissipation in the channel is Joule heat, which depends on the current in the channel. The main components of the channel are the drift current  $J_{dr}$ , the diffusion current  $J_{dif}$ , and the thermic current  $J_t$ . To understand the impact of geometrical and physical parameters on SHE, we consider nanoscale JLFinFETs of both transistor groups.

#### 3.1. Performance analysis of nanoscale JL FinFET with rectangular channel

The resulting current density in the middle of the channel for different  $T_{Si}/W_{Si}$  is shown in Fig. 4a. Fig. 4b shows the simulation result of the electric field dependence on  $T_{Si}/W_{Si}$ , concentration, and temperature gradient for the different ratios of  $T_{Si}/W_{Si}$  shown in Fig. 4c.

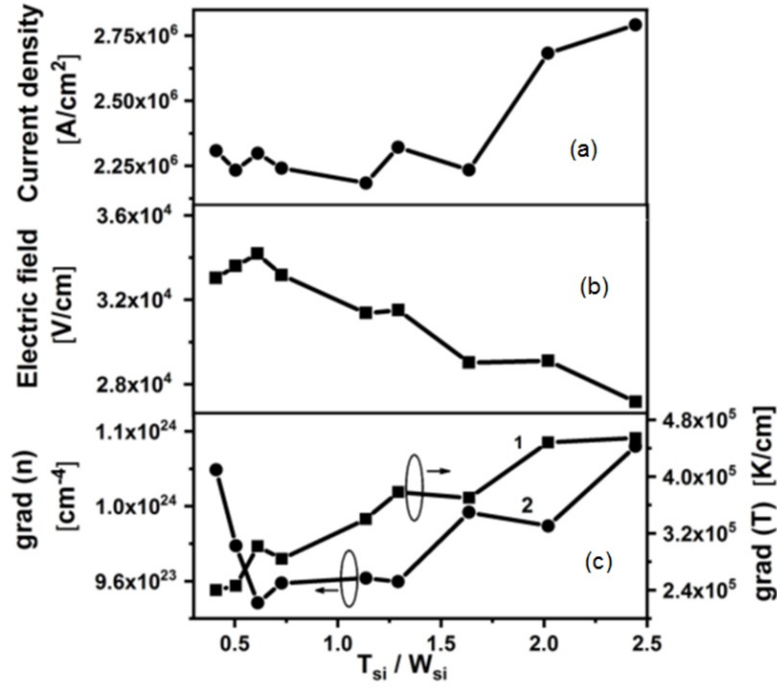


FIG. 4. (a) current density, (b) electric field, (c) concentration gradient (curve 1), and temperature gradient (curve 2) as a function of  $T_{Si}/W_{Si}$  in the center of the channel

The dependences shown in Fig. 4 were carried out from the distribution of the field, concentration, and temperature along the center of the channel. Typical distributions, for example for  $T_{Si}/W_{Si} = 0.4$  are shown in Fig. 5. Based on the dependences shown in Fig. 4 all types of density currents were estimated. For example, for  $T_{Si}/W_{Si} = 1.3$ , the densities of drift current ( $j_E$ ), diffusion current ( $j_{\Delta n}$ ), and thermal current ( $j_{\Delta T}$ ) are calculated from equations (1)–(3):

$$j_E = en\mu E, \quad (1)$$

$$j_{\Delta n} = eD \frac{\Delta n}{\Delta x}, \quad (2)$$

$$j_{\Delta T} = \sigma S \frac{\Delta T}{\Delta x}. \quad (3)$$

In equations (1)–(3),  $e$  is the elementary charge,  $n$  stands for the carrier concentration,  $\mu$  represents the electron mobility,  $D$  is the diffusion coefficient of electrons in silicon,  $\sigma$  the conductivity of silicon, and  $S$  stands for the Seebeck coefficient for silicon.

The calculation has led to the values  $j_E = 6.98 \cdot 10^6$  A/cm<sup>2</sup>,  $j_{\Delta n} = 4.83 \cdot 10^6$  A/cm<sup>2</sup>, and  $j_{\Delta T} = 3.78 \cdot 10^2$  A/cm<sup>2</sup>. It is observed that the thermal current density is several orders of magnitude lower than the other two types of current density. It can therefore be taken into account that the main contribution to the resulting current density has a drift current (lower inset in Fig. 5) and a diffusion current (upper inset in Fig. 5), which have the same order of values.

In Fig. 5, it can be seen that the concentration gradient has two components with opposite directions and different values. This is related to the different influences of the normal (vertical) gate field at the source and drain end on the drain current. In fact, one component is directed along ( $J_{n+}$ ) and the second one is directed opposite ( $J_{n-}$ ) to the field between source and drain (upper insertion in Fig. 5). The estimations show that the resulting diffusion current ( $J_n = J_{n+} - J_{n-}$ ) is directed opposite to the drift current. The resulting channel current is therefore defined as the difference between the drift and the resulting diffusion current.

A comparison of the dependencies in Fig. 4 shows that the increase in the current density at a high  $T_{Si}/W_{Si}$  is due to an increase in the diffusion current. It can be seen that the current density is increased for transistors with  $T_{Si}/W_{Si}$  greater than 1.75, while the lattice temperature in the middle of the channel increases monotonically in all ranges with increasing  $T_{Si}/W_{Si}$  (Fig. 6), which is not appropriate to the current density dependence on  $T_{Si}/W_{Si}$ .

Our findings allow the conclusion that the resulting current density in the channel is not only the main factor for the dependence of the lattice temperature on the channel shape. It is mainly related to the structure's capability/ability to dissipate heat and not just to the power of the heat source. The main routes for heat dissipation from the center of the channel are through the back oxide layer and the gate oxide layer. These heat dissipation capabilities can be expressed by the formula (see Eq. (4)) of the dependence of the temperature change in a channel on the thickness of the back oxide

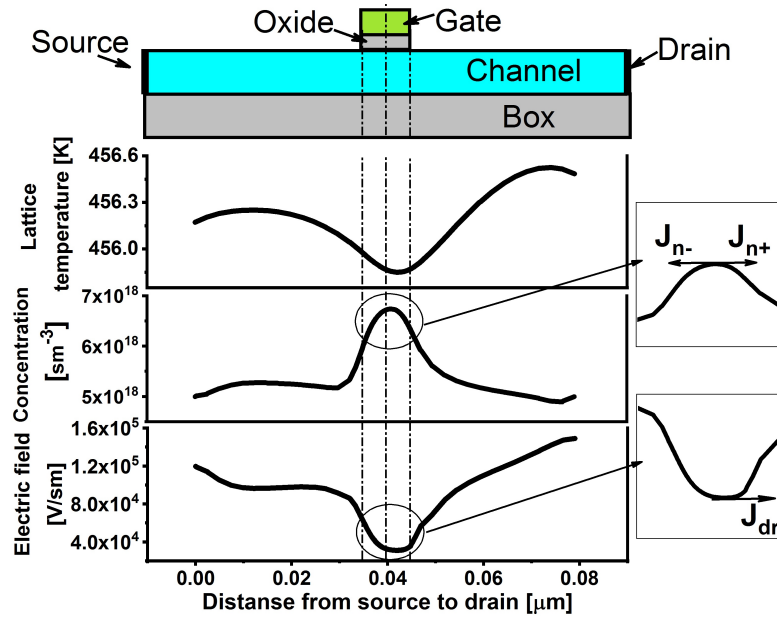


FIG. 5. Typical distribution of the temperature, electron concentration, and the field along the middle of the channel.  $T_{Si}/W_{Si} = 0.4$

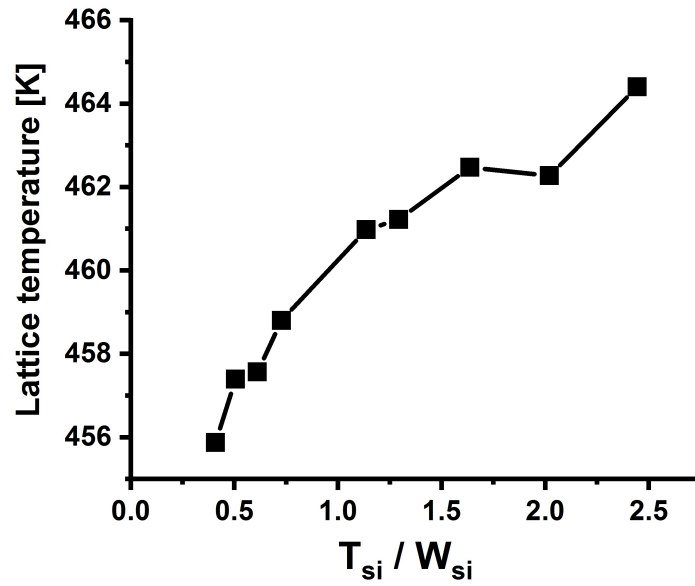


FIG. 6. Dependence of the temperature in the middle of the channel on the ratio  $T_{Si}/W_{Si}$  for transistors of the first group

layer, proposed in [23]:

$$\Delta T = \frac{(P_t \cdot T_{ox})}{K_b \cdot A}, \quad (4)$$

where  $P_t$  stands for the heat power generated by current in the channel,  $K_b$  is the heat conductance of the oxide layer, and  $A$  represents the area of the contact surface between the oxide layer and the channel. To compare the heat dissipation through back oxide and gate oxide layers, we used equation (4) for both gate oxide and back oxide layers. From equation (4), the gate oxide is justified, because the physical mechanism of heat dissipation through the back oxide and gate oxide are the same. For the back oxide layer  $A = W_{Si} \cdot L$  and gate oxide layer  $A = (2T_{Si} + W_{Si}) \cdot L$ , where  $L$  stands for the channel length. Therefore, when using the independent heat dissipation through the oxide layers, the temperature changes associated with the heat dissipation through the back oxide layer and gate oxide layer, normalized to the heat power, can be written from (4) using the following formulas:

$$\frac{\Delta T}{P_t} = \frac{T_{box}}{K_{box} \cdot W_{Si} \cdot L}, \quad (5)$$

$$\frac{\Delta T}{P_t} = \frac{T_{gox}}{K_{gox} \cdot (2 \cdot T_{Si} + W_{Si}) \cdot L}, \quad (6)$$

where,  $T_{box}$  is the thickness of the back oxide layer,  $T_{gox}$  represents the thickness of the gate oxide layer,  $K_{box}$  and  $K_{gox}$  are the heat conductivity of the back and gate oxide layers, respectively. For these two heat dissipation mechanisms, the  $\Delta T/P_t$  dependence on  $T_{Si}/W_{Si}$  (channel shape) is presented in Fig. 7. For simulation, we considered SiO<sub>2</sub> as the back oxide layer and HfO<sub>2</sub> as a gate oxide. The heat conductance of the hafnium oxide layer is in the range from 0.49–0.95 W/(m·K) in the temperature range from 300–500 K, and the heat conductance of SiO<sub>2</sub> is in the range from 1.2–2 W/(m·K) in the temperature range from 200–1500 K. In the simulation we used the value of the heat conductance 0.6 for HfO<sub>2</sub> and 1.5 for SiO<sub>2</sub>. As it appears from Fig. 7, a big gap in the values of heat conductances results in a higher heat dissipation through the back oxide layer. The curve of the  $\Delta T/P_t$  dependence on  $T_{Si}/W_{Si}$  for the back oxide layer (Fig. 7, curve 1 (SiO<sub>2</sub>)) grows monotonically like the  $T$  dependence on  $T_{Si}/W_{Si}$  depicted in Fig. 6. At the same time, during the heat dissipation through the gate oxide, the  $\Delta T/P_t$  slowly decreases with increasing  $T_{Si}/W_{Si}$  (insertion in Fig. 7). This testifies to the main role played by the back oxide layer in heat dissipation and temperature setting in the center of the channel.

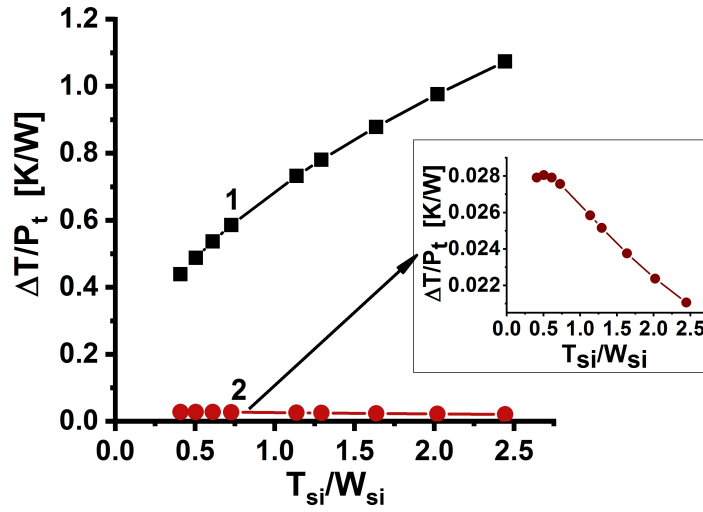


FIG. 7.  $\Delta T/P_t$  dependence on  $T_{Si}/W_{Si}$  in cases of the heat dissipation through back oxide (curve 1) and gate oxide (curve 2) layers for the transistors of the first group

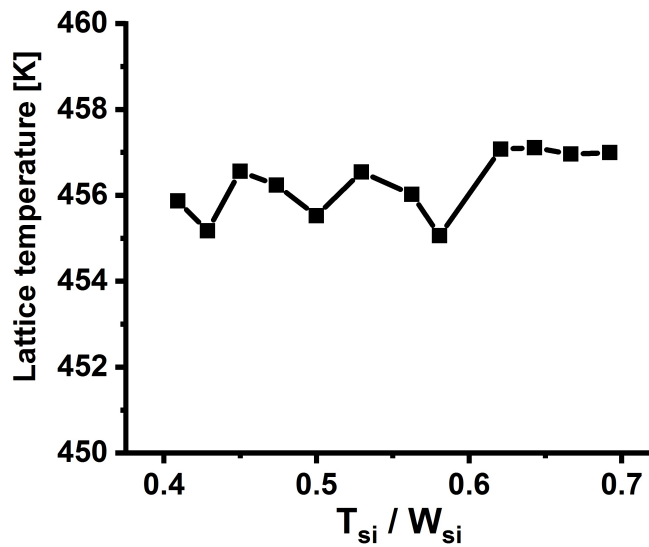


FIG. 8. Dependence of the temperature in the middle of the channel on the ratio  $T_{Si}/W_{Si}$  for transistors of the second group



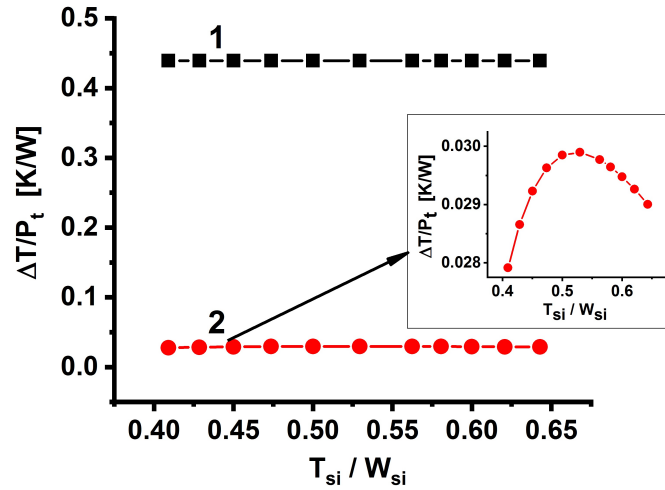


FIG. 9.  $\Delta T/P_t$  dependence on  $T_{Si}/W_{Si}$  in cases of the heat dissipation through the back oxide (curve 1) and gate oxide (curve 2, inset) layers for the transistors of the second group

### 3.2. Performance Analysis of nanoscale JL FinFET with different channel shapes

In order to define the role of back and gate oxide layers in SHE in transistors with different channel cross-sections, the temperature dependence (in the channel center) on  $T_{Si}/W_{Si}$  was simulated for transistors of the second group. With transistors of this group, the channel width and the channel cross-sectional area are constant, while the cross-sectional shape changes from rectangular to trapezoidal shape (Fig. 2). In this case, the values of  $T_{Si}/W_{Si}$  can be changed only in the range from 0.4 up to 0.7. The results of the simulation are shown in Fig. 8. It can be seen that the temperature in the center of the channel is practically unchanged. This is associated with a constant channel base width while the cross-sectional shape is changed. In the case of heat dissipation through the back oxide layer,  $\Delta T/P_t$  practically does not change with the increase in  $T_{Si}/W_{Si}$ , as shown in Fig. 9. In the case of heat dissipation through the gate oxide layer, the  $\Delta T/P_t$  dependence on  $T_{Si}/W_{Si}$  does not have a monotonic character (inset in Fig. 9). The underlined dependence does not correspond to the temperature dependency in the center of the channel on the channel cross-sectional shape. Therefore, in this case too, a back oxide layer plays the main role in heat dissipation.

## 4. Conclusions

The above results revealed that for nanoscale JL FinFET with the different channel cross section shapes and with a defined thickness of back and gate oxide layers, the main factors that define the temperature at the center of the channel are the thermal conductivity of the oxide materials and the contact surface area between the channel and the oxide layers. In the case of transistors with  $\text{SiO}_2$  as the back oxide layer and  $\text{HfO}_2$  as the gate oxide layer, the temperature in the channel center is mainly defined by the width of the channel base in contact with the back oxide layer. Considering an increase in the  $T_{Si}/W_{Si}$  ratio with a constant channel cross-sectional area, the channel temperature rises, which is associated with a reduction in the channel base width of a transistor with a rectangular cross-section. Therefore, when considering the channel shape for nanoscale JL FinFETs, in order to reduce the SHE and obtain a more reliable nanoscale device, the main focus should be given to the contact surface between the channel and the oxide layers.

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