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Original article

Influence of SiC MOSFET design on on-resistance and breakdown voltage

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ABSTRACT To improve the efficiency of circuits including SiC MOSFET, it is necessary to increase their specific currents and reliability, respectively. One needs it to reduce the transistor on-resistance and to increase its breakdown voltage. To achieve these goals, the influences of the transistor's electrophysical characteristics on its design and technological features have been studied with Sentaurus TCAD. We showed that for increasing the transistor currents, it is necessary to reduce the channel length – the distance between the p-bases of the transistor sources, and to create a JFET region. For the increasing the breakdown voltage of the device, we proposed to increase the doping level of the drift region, and suggested a new transistor design that will allow one to obtain devices with a breakdown voltage up to 2500 V.

KEYWORDS SiC MOSFET, TCAD, JFET doping, breakdown voltage.

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1. Introduction

Nowadays, many devices are formed on silicon wafers, particularly, devices for power applications. IGBT silicon transistor is the most applicable for power electronics since it has higher breakdown voltages and operating temperatures compared to other types of silicon devices. It is difficult to achieve a high power conversion factor using Si devices [1]. The most suitable devices for power applications are based on wide-bandgap materials [2], such as gallium nitride, silicon carbide or gallium oxide. SiC compared to Si has larger bandgap width – 3.26 eV, higher thermal conductivity – 4.9 W / cm·K, and higher value of the critical electric field strength of breakdown – 3 MV / cm.

Power MOSFETs can be lateral or horizontal. Power lateral devices must have a wide drift area to withstand high voltages, i.e. the cell size must be large. Vertical transistors don't require wide drift areas, that allows one to reduce the cell size and also solve the problem of large electric field on the surface.

Standard Si MOSFETs have breakdown voltages of less than 150 V [3] and there are many such offers from different companies. However, there is now a trend to increase the values of the device's operating voltages and breakdown voltages. Vertical silicon carbide devices have high breakdown voltages, high radiation resistance, low on-resistance and excellent switching frequencies compared to silicon-based devices therefore they are more attractive for power applications. The main researches in this area are aimed on improving their characteristics, namely, the breakdown voltage Vbd, the channel resistance Ron,sp, the gate charge Qg and the maximum electric field in the gate dielectric Emax,ox [4–7].

Standard SiC MOSFETs have breakdown voltages in the range of 600 to 900 V and threshold voltages up to 10 V [8]. At breakdown voltages below 1000 V, the performance of SiC devices is strongly dependent on the on-resistance as well as the charge carrier mobility. If the charge carrier mobility is approximately 100 $cm^2/V{\cdot}s$, the on-resistance becomes almost equal to the ideal value when the breakdown voltage exceeds 5000 V. Even at high breakdown voltages, if the charge carrier mobility reaches values of 10 $cm^2/V{\cdot}s$, the performance of SiC devices deteriorates [9]. Therefore, it is necessary to create transistor designs with low on-resistance and high breakdown voltages.

Nowadays, a sufficient number of different designs of power SiC MOSFETs have been developed in order to improve the listed characteristics: SiC Power DI-MOSFET (Double-Implant Process) [10], Shielded SiC Planar Power MOSFET [11, 12], MOSFET with spreading layer or/and JFET region that solves the problem of low on-resistance [13], ACCUFET structure with epitaxial layer N-base region under the gate [14, 15], JBSFET with integrated JBS diode [16, 17], Bi-directional FET – 2 JBSFET with common drain [18, 19], trench-gate MOSFET or/and JFET region [20] etc. Shielded SiC Planar Power MOSFET has a shielded layer under source and base that solves a reachthrough problem, problem of a high gate oxide electric field and low channel mobility. But all the listed designs allowed obtaining devices with breakdown voltage in the range from 1000 to 1650 V. One work reflects the formation of an ACCUFET with a breakdown voltage of about 10 kV, but its threshold voltage was approximately zero.

In this paper, we study the design and technological features of a standard power MOSFET using physical simulation in the Sentaurus Technology Computer Aided Design (TCAD) and the transistor design to reduce channel resistance Ron,sp and increase the breakdown voltage Vbd.

2. Structure

Fig. 1 demonstrates a schematic image of the SiC MOSFET. The values of the layer thicknesses and their concentrations are standard for such structures [21–24]. When a bias is applied between the drain and source Vds, and the gate-source voltage Vgs is greater than the threshold voltage Vth, the transistor opens and a vertical current exists between the drain and the source. If the gate-source voltage Vgs is less than the threshold Vth, and the bias Vds is still applied between the drain and the source, then there is no current, the transistor is closed, the drift region is depleted, and an electric field begins to be induced. Breakdown occurs when the value of the induced electric field exceeds the critical value as the bias between the drain and the source increases.

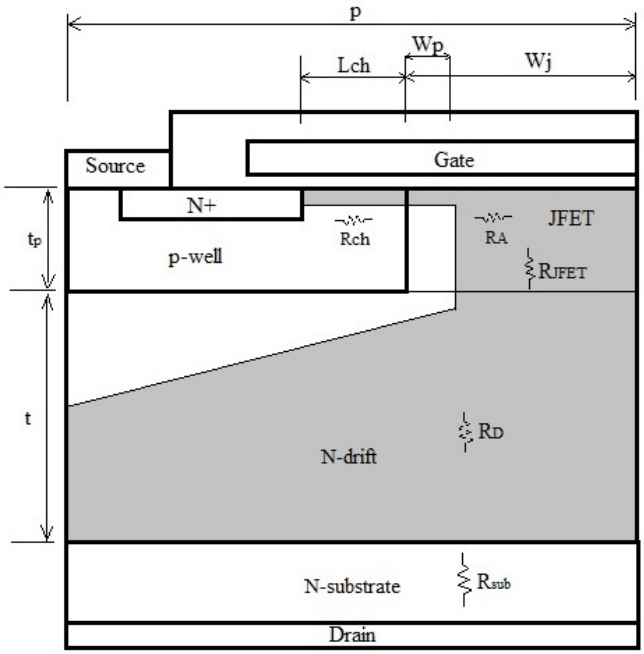

FIG. 1. Schematic image of SiC MOSFET, tp – width of p-region, t – drift region width, p – half length of the structure, Lch – channel length, Wp – width of p-n junction p-base/N-JFET, Wj – JFET region width

3. Simulation

The study of the design and technological features of SiC power MOSFETs has been carried out using the Sentaurus TCAD. Two-dimensional simulation of the structure has been carried out. To save time half of the structure was considered during simulation since the device is symmetrical relative to the vertical axis, therefore, to compare it with the real device the results of simulation drain currents, for example, should be increased twice.

The first step of the device simulation is to describe the structure, then you should form the device grid in the nodes of which such electrophysical characteristics of the device as electric field, voltage, current, etc. will be calculated using numerical calculations. The number of nodes in the grid affects the modeling process, namely, the accuracy of the results, as well as the convergence of the problem. If the number of nodes is small, i.e. a so-called "rough" grid has been generated, the result may be inaccurate. If the number of nodes is large and the grid is very "fine", the problem may not converge or the simulation time will be too long. Therefore, it is important to select the optimal number of grid nodes. For the accuracy of the results, it is necessary to generate a "fine" grid only in the areas of heterojunctions, channel, concentration gradient, etc.

The key model in simulation of devices is the diffusion-drift model, which is based on the approximation of the Boltzmann charge transport equation in the diffusion-drift approximation. The current in the device flows due to the drift and diffusion of charge carriers simultaneously with their generation and recombination. The diffusion-drift model numerically solves the Poisson equations and calculates the concentrations of electrons and holes, and determines the electrostatic potential at each grid node. A thermodynamic model is often also included. The influence of temperature on

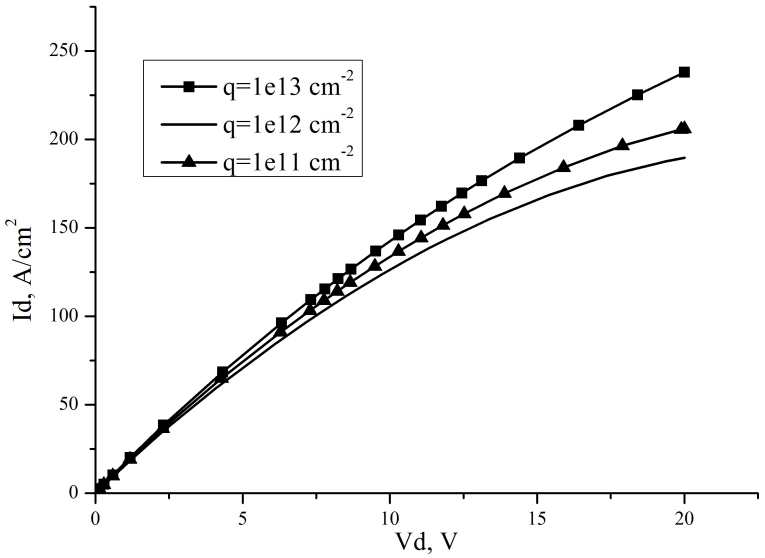

FIG. 2. The influence of positive charge density q at SiO_2/SiC heterojunction on MOSFET current-voltage characteristics at 20 V gate voltage

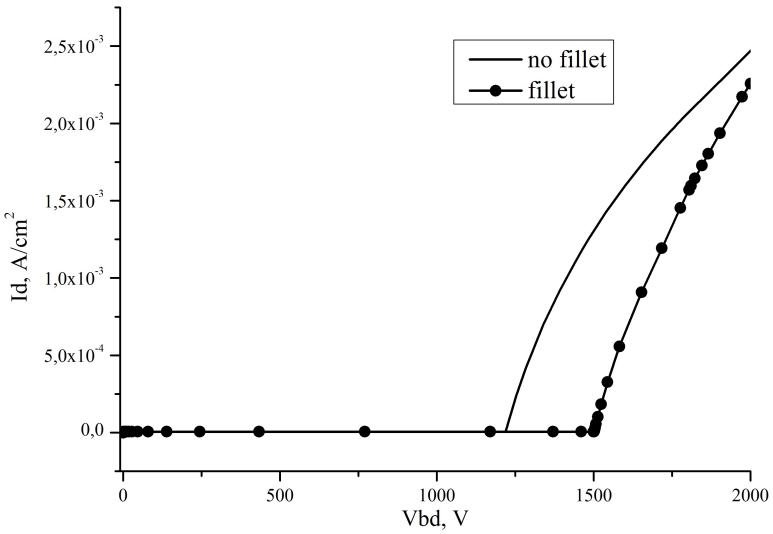

FIG. 3. Influence of drain p-region describing on SiC MOSFET breakdown voltage

the parameters of the device is taken into account. If it is included then the heat flow equations are additionally solved, i.e. the temperature gradient in the device is taken into account.

The physical model of the transistor should take into account the recombination and carrier generation. These are the processes of creation and destruction of an electron-hole pair by the transition of an electron from the valence band to the conduction band, thereby creating a hole in the valence band, and vice versa. The difference in energies between the final position of the electron and the initial one leads to different classifications of the recombination process. If the radiative recombination energy is released in the form of a photon and in the case of nonradiative recombination, it is transferred to one or more phonons.

The key model of recombination and generation is the Shockley-Read-Hall model. The Shockley-Read-Hall model describes the process of electrons and holes recombination through the trap levels in the forbidden band. An electron moves from the valence band to the trap level and then from this level to the conduction band. This process occurs in a semiconductor due to the presence of impurities and defects formed during the growth [22].

Auger recombination model should be included at simulation of power SiC MOSFETs that have high drain currents. Auger recombination is an interband transition of an electron or a hole. The energy released during such a transition is transferred to another electron or hole that affects the recombination rate [23].

Incomplete ionization models and band gap narrowing model should be also used since the dopant in 4H-SiC isn't completely ionized at room temperature. Doping dependence mobility and high field saturation mobility models have

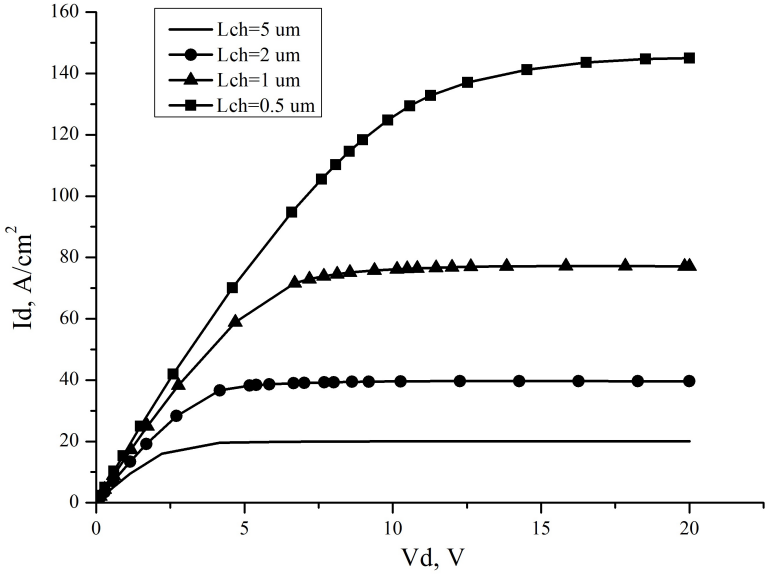

FIG. 4. Influence of length channel Lch on the transistor current-voltage characteristics at 15 V gate voltage

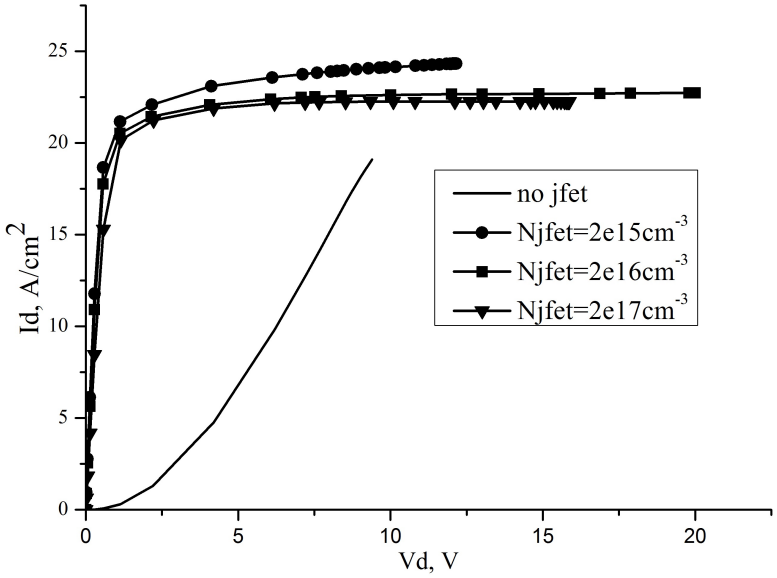

FIG. 5. Dependence of current-voltage characteristics on doping concentration of JFET region Njfet at 15 V gate voltage

been used to calculate the mobility. An avalanche model, i.e. impact ionization model, should also be used to simulate breakdown voltage.

One of the advantages of SiC for practical application is the formation of insulating silicon oxide layers SiO_2 on SiC by thermal oxidation. This effect is important for the fabrication of field-effect MOSFETs. There are two types of oxidation processes: dry and wet. The dry oxidation process of SiC is carried out in an O_2 atmosphere. The wet oxidation process is carried out in an O_2 and H_2O atmosphere and it effectively reduces the influence of deep trap levels on the SiO_2/SiC heterojunction, which improves the channel mobility of the MOSFET [24, 25]. Therefore, the effect of this charge on the transistor electrical characteristics has been studied (Fig. 2). Based on the literature data [26], the value of this charge is about 10^{11} cm^{-2}. The influence of this charge on the drain current at the same gate voltage is weak. Therefore, in our case a charge of $1{\cdot}10^{11}$ cm^{-2} was set on the heterojunction.

It is necessary to describe the fillet of the p-doped region simulating such devices. If this is neglected the maximum electric field strength at breakdown voltage simulation will be concentrated at corner of the p-region. It will lead to incorrect results and a decrease in the breakdown voltage from 1500 V to 1200 V for the research structure heterostructure (Fig. 3).

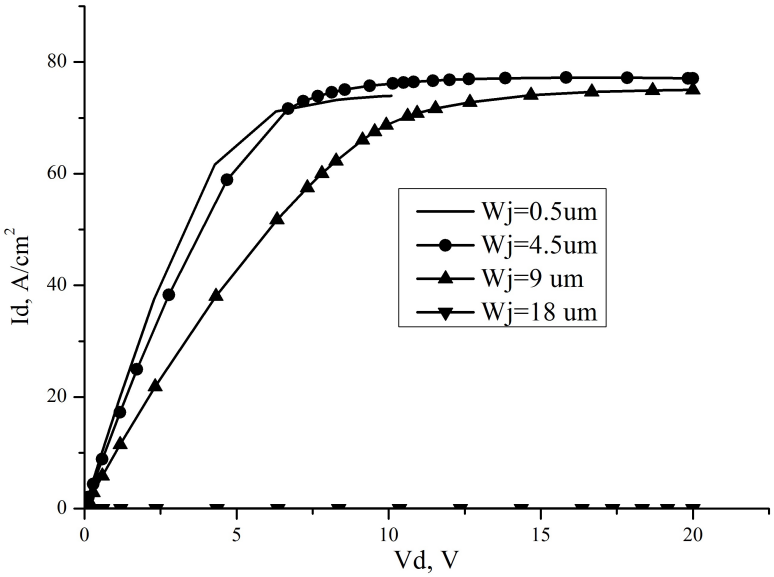

FIG. 6. Influence of JFET region width Wj on current-voltage characteristics at 15V gate voltage

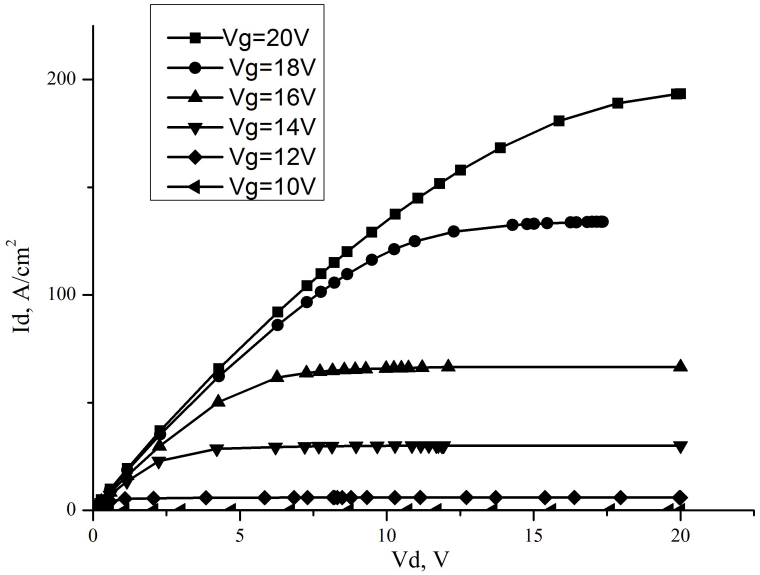

FIG. 7. Current-voltage characteristics of the SiC MOSFET

4. On-resistance

One of such devices research directions is to reduce on-resistance. The most popular approach is to dope the region under the gate between the p-type regions [27]. This region is named as a JFET. JFETs are usually formed by implanting high-energy nitrogen ions with a concentration of about 10^{17} cm^{-3} [28]. In the open state, the current through the transistor begins to flow through the inversion layer, which is formed in the upper part of the p-type region due to the positive bias. This is so-called channel. The current then flows through the JFET region and then spreads into the drift region, in which the current flow region also extends under the p-type region at an angle of 45° (gray region in Fig. 1) [9]. The total on-state resistance of the transistor can be calculated using the following formula:

$$R_{on} = R_{ch} + R_A + R_{jfet} + R_{drift} + R_{subs},$$

where R_{ch} is the channel resistance, R_A is the resistance of the p-n junction, R_{jfet} is the resistance of the JFET region, R_{drift} is the resistance of the drift region and R_{subs} is the resistance of the N+ substrate.

The on-resistance depends on the channel length Lch or the structure length p. The longer the channel length or the structure length, the greater the channel resistance. The influence of the channel length on the drain current was simulated

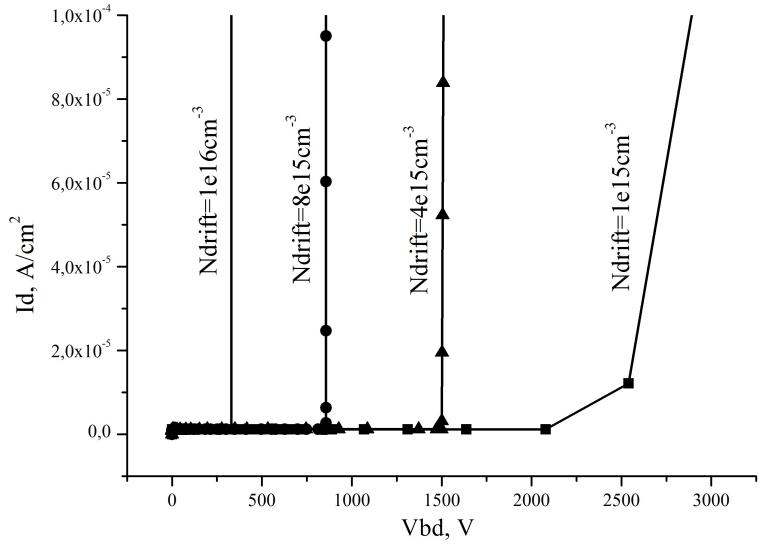

FIG. 8. Dependence of SiC MOSFET breakdown voltage on drift region doping concentration Ndrift

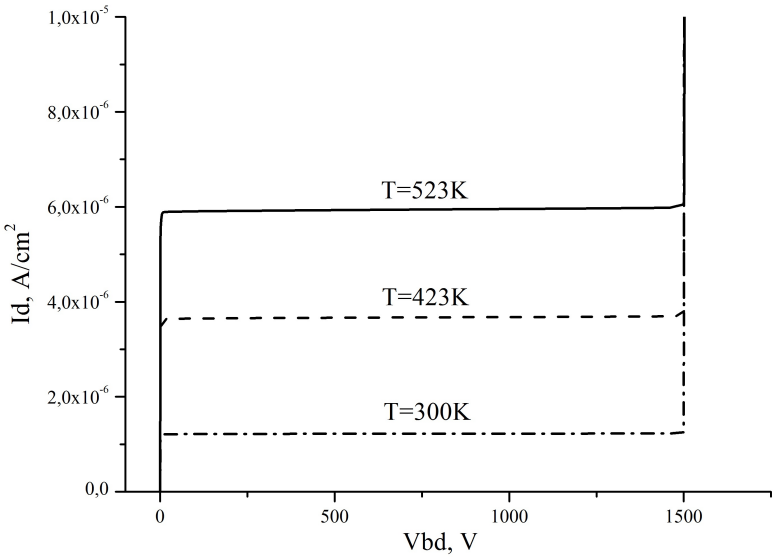

FIG. 9. SiC MOSFET breakdown voltage at different temperatures

(Fig. 4). Increasing the channel length, the resistance of the channel region also increases, which leads to a decrease of the drain current. Therefore, the optimal transistor channel length is about 0.5–1 μm.

The p-n heterojunction resistance R_A depends on p-base/N-JFET junction width W_p at zero bias and on the JFET region width. In turn, the width W_p depends on the dopant concentration of the JFET region. The resistance of the JFET region is determined by the parameters of the p-base, the width of the JFET region and the width W_p. The resistance of the drift region also depends on the base parameters and the parameters of the JFET region. If the typical values of the resistance for 4H-SiC substrate are 0.02 $\Omega\cdot$ cm and 350 μm, then the resistance is equal to $7\times10^{-4}\Omega\cdot$cm^2 [29].

Obviously, the transistor resistance is greatly affected by the dopant concentration of the JFET region, as well as the length of the structure. Therefore, the dependences of the transistor drain current on the JFET region dopant concentration N_{JFET} and the width of this region L_S were investigated. Fig. 5 demonstrates that the JFET region doping reduces the transistor resistance, but the dopant concentration has small effect on the drain current value. The larger the width of the JFET region *Wj*, the lower the resistance and the higher the drain current (Fig. 6). Therefore, JFET region with a width of approximately in the range from 0.5 to 9 μm should be created in the device to reduce the transistor resistance.

Thus, the following SiC MOSFET design was chosen: the distance between the p-regions Wj is about 9 μm, the channel length Lch – 1 μm, the thickness of the p-region tp 5 μm, the drift region width t – 25 μm, the doping concentration in the source region N^+ is 1.5e20 cm^{-3}, the doping concentration in the p-region - 4e17 cm^{-3}, the doping concentration in the drift region *Ndrift* = 4e15 cm^{-3} and the JFET concentration is 2e16 cm^{-3}. For this transistor current-voltage

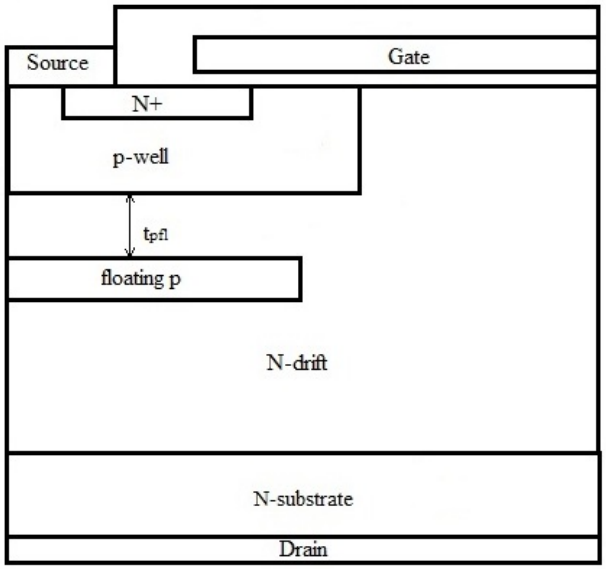

FIG. 10. Schematic image of SiC MOSFET with additional p-region in the drift region to increase the breakdown voltage

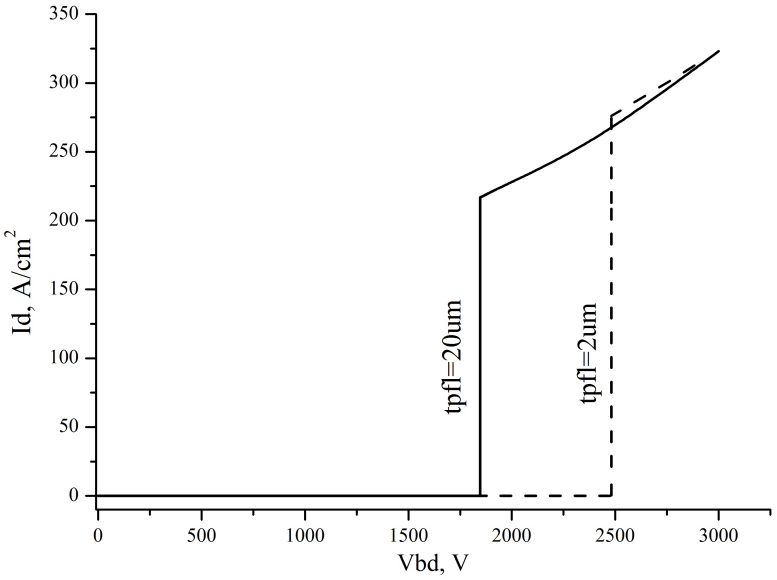

FIG. 11. Breakdown voltage of SiC MOSFET with additional p-region in drift region with different distances from p-base to additional p-region tpfl

characteristics were simulated (Fig. 7). The threshold voltage was 10 V, and the maximum drain current at 20 V on the gate was 192 A/cm^2. To obtain a higher transistor current the channel length or the distance between the p-regions should be reduced. The purpose of our work is to study the design and technological features of SiC MOSFET, so we consider the standard design and offer ways to improve the electrophysical characteristics of the device. Let us consider in more detail the methods for increasing the breakdown voltage of SiC MOSFET.

5. Breakdown voltage

The breakdown voltage of the research SiC power transistor depends on the doping concentration of drift region and on its width [30]. It was found that the value of the breakdown voltage weakly depends on the drift region width SiC transistors with different drift region widths (20, 25, 30 and 35 μm) have been simulated. The breakdown voltages of the studied SiC transistors with different draft region widths were 1510 V, 1498 V 1518 V and 1493 V accordingly. However, the doping concentration of the drift region has a strong effect on the breakdown voltage value. The lower the concentration, the higher the breakdown voltage takes place (Fig. 8).

The influence of temperature on the breakdown voltage was investigated (Fig. 9). The breakdown voltage of the device was 1500 V. The drain current increases at the same drain voltage values with increasing temperature, and the breakdown voltage doesn't change. This can be explained by the fact that holes have higher temperature coefficient in SiC [31], and accordingly, they have a higher ionization rate compared to electrons, so the breakdown voltage doesn't change. Despite the fact that there are many additional holes, electrons remain the main carriers.

As mentioned above, one of the key goal of SiC MOSFET study is to increase the breakdown voltage. One of the ways to solve this problem is to increase the doping level of the drift region. In this paper, we also propose a transistor design with an additional p-region in the drift region (Fig. 10). This p-region extends the peak of the breakdown electric field, which allows increasing the breakdown voltage. It is possible to obtain transistors with different breakdown voltages by changing the distance from the p-base to the additional p-region t_{pfl}: at 2 μm, the transistor has a breakdown voltage of 2475 V, and at 20 μm – 1845 V (Fig. 11).

6. Conclusion

In this article, the design and technological features of standard SiC MOSFET transistor are stuydied and the process of simulation such devices in the Sentaurus TCAD are described in detail. To reduce the on-resistance of such transistors, and, accordingly, to increase the drain currents, it is necessary to form the JFET region between the p-bases of the sources. Also, to increase the current, it is possible to reduce the channel length to 0.5–1 μm or reduce the width of the JFET region. The distance between the p-bases of the sources should be less than 9 μm. To increase the breakdown voltage of power SiC MOSFET, it is necessary to reduce the concentration of the dopant in the drift region: at the concentration of 1e15 cm^{-3}, a breakdown voltage of 2500 V can be obtained. In order to increase the breakdown voltage, a new design of power SiC MOSFET with an additional p-region in the drift region is proposed. By varying the distance from this p-region to the p-base, it is possible to obtain transistors with the breakdown voltages of various values up to 2500 V.

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Conflict of interest: the authors declare no conflict of interest.