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Negative differential resistance in gate all-around spin field effect transistors

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In this paper, novel gate all-around spin field effect transistors (GAA Spin-FETs) with three different channel materials are proposed and their transport properties are presented. The three channel materials used are Indium Arsenide (InAs), Indium Phosphide (InP) and Aluminum Antimonide (AlSb). Based on the type of semiconducting channel, the results are obtained and a comparison of transport properties among these three FETs is made. The proposed device offers both advantages of reduced power dissipation and compact size. The results reveal that the negative differential resistance (NDR) is observed in all modeled devices and the peak to valley current ratio (PVCR) is different in all structures and is maximum in AlSb based field effect transistor. It is expected that these results will find enormous applications in analog electronics and in the design of oscillators. Additionally, the observed results in this study have great potential for the design of various logic gates and digitals circuits.

Keywords: Spin-FET,gate all-around spin field effect transistors, multi-gate FETs, NDR, datta-das transistor.

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1. Introduction

Spin-based devices promise to be a technology of beyond-CMOS computing [1]. Various spin devices have also been proposed and studied for various applications, such as two-terminal giant magnetoresistance (GMR) and tunneling magneto-resistance devices (TMR), which find applications in designing non-volatile spin based RAMs called STT-RAM (spin transfer torque random access memory) [2]. Spin field effect transistor (Spin-FET) is believed to be a better device than conventional semiconductor field effect transistor devices due to its exceptional properties, such as control of conductivity using spin degree of freedom [3]. Owing to less energy required for control of spin, Spin-FET is well suited for low-power applications, and hence, can resolve the power issues of conventional transistors [4]. Spin-FET was proposed by S. Datta and B. Das in the year 1990 and has appeared as one among the mostly researched device for various applications [5]. Spin-FET differs from the conventional MOSFET in structure, as the conventional MOSFET has semiconductor material-based source and drain terminals, while spin-FET has ferromagnetic material based source and drain electrodes [5]. Since there are various ferromagnetic materials like iron, cobalt and nickel, thus there is a choice of using the material of desired magnetic properties for a particular device [6].

The spin-FET works on the principle similar to that of conventional MOSFET, with the difference being that spin-FET only allows the electrons with one desired polarization and rejecting all other electrons with other polarizations [7]. The main function of using ferromagnetic source is to spin polarize the source current, the gate voltage rotates the orientation of the injected spins in the current by an angle that depends on the gate voltage (because of the Rashba effect induced by the gate voltage in the channel) [8]. The drain acts as a filter that preferentially transmits spin of one polarization and blocks spins of the opposite polarization [9], [10]. The added advantage in the proposed device is that gate all-around structure is used, and has the better control over the flow of electrons through the channel [11].

Various types of gate all-around field effect transistors (GAA-FETs) have been studied in the open literature over the past several years [12–16]. For example, in 2016, the negative differential resistance (NDR) was obtained in a boron nitrogen co-doped axial carbon nanotube field effect transistor [12], whereas NDR is observed in a molecular junction of carbon nanotube and benzene [13]. In 2012, R. Grassi et al [14], exploited NDR in monolayer graphene FETs for high voltage gains and in 2013 A. Sengupta et al [15], reported negative differential resistance behavior in MoS_2 armchair nanoribbon MOSFETs. Moreover, Y. Wu et al [16], have experimentally demonstrated prototypes of novel three-terminal graphene NDR device and provided an analytic model to elucidate such NDR behavior.

Compared to the devices presented in [12–16], where the different materials and methods are used which may not be compatible with existing technology, the most important advantage of our proposed device is that it has no compatibility issue with the existing silicon technology. In addition, its fabrication process is also feasible. The

proposed device is simply an addition of a gate stack to the magnetic tunnel junction (MTJ). In recent years MTJs have been commercially fabricated, thus this advantage can be exploited which makes the proposed device more feasible to be fabricated. Later the channel materials have been changed from InAs to InP to AlSb.

A total of 14 molecules were used for semiconducting channel materials. The value of the lattice constants for the Indium Arsenide (InAs), Indium Phosphide (InP) and Aluminium Antimonide (AlSb) are 0.60 nm, 0.58 nm and 0.61 nm respectively. Hence the channel length is determined to be approximately 20 nm. The channel material length affects the performance of GAA Spin-FET. In order to accommodate a greater number of devices on a single chip, the channel length is scaled down, which reduces the device dimensions. However, the decrease in channel length leads to deterioration of the performance and causes second order short channel effects. Thus, in order to have sufficiently large number of devices on a single chip as well as satisfactory performance, the channel length is chosen in mid-range i.e., 20 nm.

In this paper, the gate all-around spin-FET is proposed and analyzed for the first time as per the authors' best knowledge. The source and drain terminals are made of cobalt, which is a ferromagnetic material. The three employed channel materials are InAs, GaAs and AlSb, as they have the potential to be used in spin-FETs. A layer of dielectric material of dielectric constant 4 is employed on the channel over which a metallic layer is made. The effects in IV-curves and conductance curves with channel materials are presented. One of the important characteristics of the modeled devices is that, they show negative differential resistance, which finds immense applications in analog electronics like high-frequency oscillators etc. Although various spin-FET devices have been reported varying in channel material as well as drain/source material, but as per authors' best knowledge, this type of spin-FET i.e., gate all around with InAs/InP/AlSb channel based spin-FETs has been studied for the first time in this paper.

The paper has been organized as: Section 2 introduces the model and methods applied for the proposed device. Section 3 introduces the simulation results and discussion. The paper is concluded in Section 4.

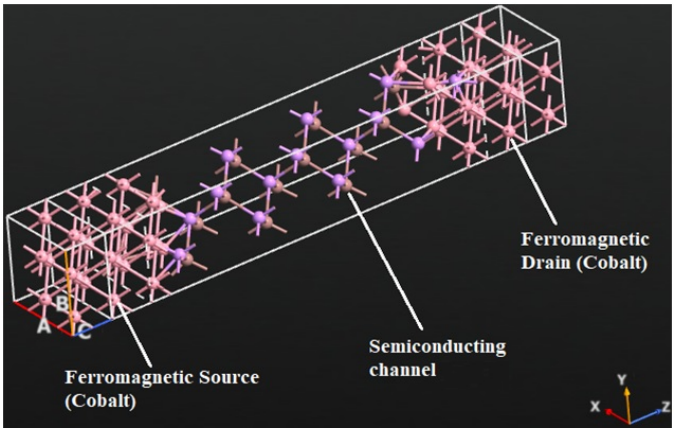
2. Models and methods

In this paper, a gate all-around spin field effect transistor (GAA-SF) is introduced. Since the drain and source regions of a Spin-FET are of ferromagnetic material, here we have used cobalt (which is a ferromagnetic material) for drain and source. The channel materials used in the proposed device are the compound semiconductors, viz., InAs, InP and AlSb. The dielectric material of dielectric constant K=4 (SiO_2) is used to insulate channel from the gate terminal. The gate terminal surrounds the channel from all the sides and forms a cylindrical gate-all around or co-axial structure as shown in Fig. 1(a) (front view without gate and dielectric material), Fig. 1(b) (cross-sectional view) and Fig. 1(c) (3D-view). The main advantage of using the gate all-around structure is symmetry along an axis is achieved, which in turn simplifies the calculations of electronic transport, and in turn, permits the self-consistent electrostatics. The proposed device has been simulated using Quantum Atomistic Tool Kit Software (version 13.8.1) [17, 18]. After building the device, it has been simulated using Extended Huckel Theory (EHT) combined with non-equilibrium Green's function (NEGF) for the calculations of transport. The temperature of electrodes has been set to 300 K. The set of k-points were selected as $1 \times 1 \times 100$ in addition of having density mesh cut-off of 100 Hartee.

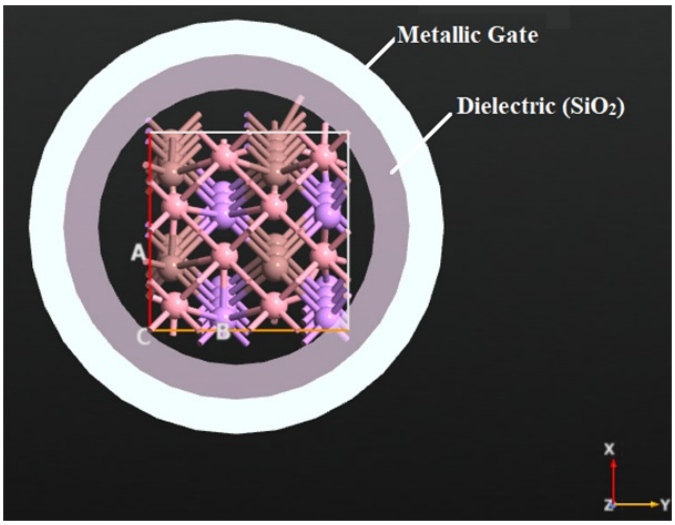
3. Simulation results

Since the device formed is due to the combination of materials having different bandgaps, consequently, a quantum well is formed. Due to this, the motion of electrons is restricted in one direction, and in such devices, within the well, a parallel transport is observed. When electrons cross the barrier (potential barrier formed due to the formation of quantum well), other transport known as perpendicular transport is observed. The perpendicular transport is a quantum mechanical phenomena due to which the negative differential resistance is observed. The proposed device has been simulated using Quantum Atomistic Tool Kit Software (version 13.8.1). The behavior of the devices is analyzed by plotting IV-curve and conductance curves for InAs, InP and AlSb based transistors. For InAs based Spin-FET, the IV and conductance curves are shown in Fig. 2(a) and Fig. 2(b) respectively, whereas for InP based Spin-FET, the IV and conductance curves are shown in Fig. 3(a) and Fig. 3(b) respectively. Fig. 4(a) and Fig. 4(b) shows the IV and conductance curves for AlSb based Spin-FET respectively.

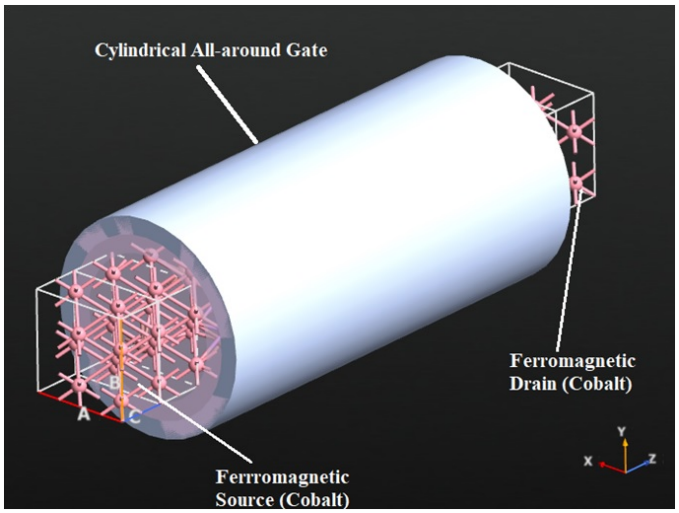
From the simulation results, it is clear that all the devices show negative differential resistance (NDR), but it can also be seen that the behavior is different while the channel material is varied from InAs to AlSb while keeping the electrodes (drain and source), oxide, gate and structure the same. It happens because of the fact the materials used for channel differ in structure and have different forbidden energy gaps. For InAs, the bandgap is approximately 0.420 eV while if we take the case of InP, the bandgap is approximately 1.421 eV and for AlSb, it is approximately 1.6 eV at 300 K temperature. Since the NDR is caused due to the band to band tunneling (BTBT) [12] and hence, it is clear that the resistance will vary as the bandgap varies.



(a)

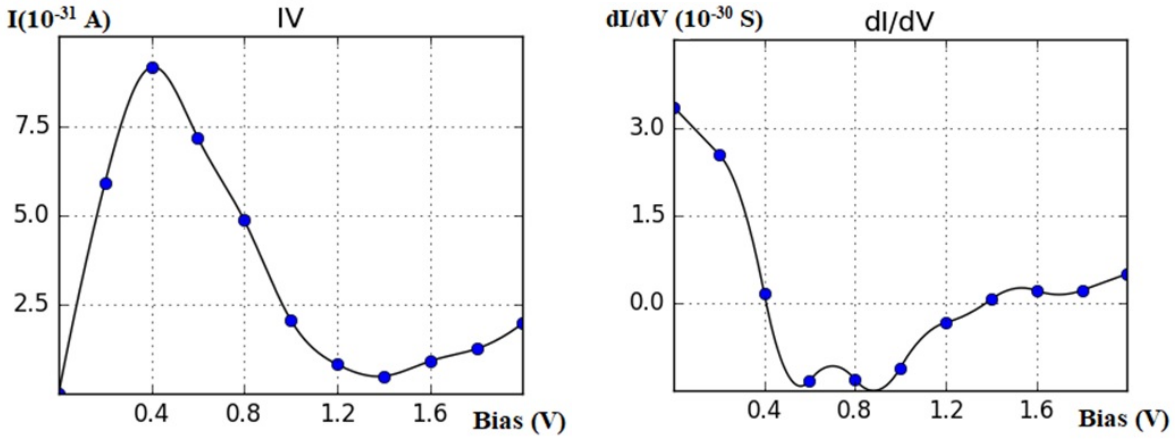


(b)



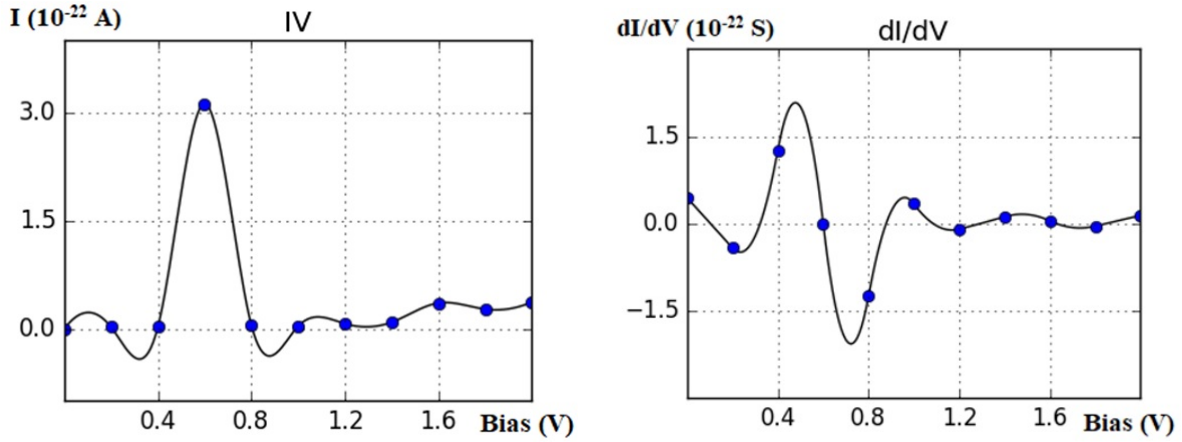
(c)

FIG. 1. (a) View of proposed device without dielectric and gate material in order to show the channel region, (b) Cross-sectional view of gate all-around spin field effect transistor (GAA Spin-FET), (c) Three dimensional (3D) view of gate all-around spin field effect transistor (GAA Spin-FET)



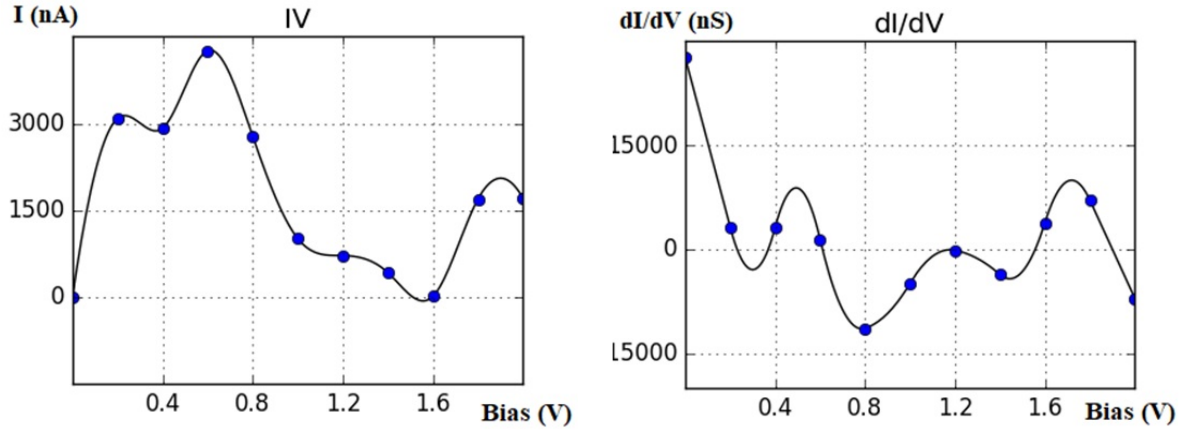
(a) (b)

FIG. 2. (a) IV-curve for GAA Spin-FET with InAs as channel material. (b) Conductance curve for GAA Spin-FET with InAs as channel material



(a) (b)

FIG. 3. (a) IV-curve for GAA Spin-FET with InP as channel material. (b) Conductance curve for GAA Spin-FET with InP as channel material



(a) (b)

FIG. 4. (a) IV-curve for GAA Spin-FET with AlSb as channel material. (b) Conductance curve for GAA Spin-FET with AlSb as channel material

In the proposed device, spin-current is evaluated in all the three different channel materials and current comes out to be in the order of 10e-31 A for InAs, 10e-22 for InP and in nA for AlSb. The changes occurred have been explained based on different bandgaps of different channel materials. However, there are several other reasons responsible for the change in current. These include spin polarization, spin detection, spin-precession and spin-relaxation. Since the source and drain material is same in all the three cases viz., cobalt (a ferromagnetic material) thus, spin polarization and spin detection will be same. However, the spin precession takes place in channel region. As the electrons of specified spin polarization move through the channel region, the spin changes without applying any voltage at the gate terminal, there exists some magnetic field like Dresselhaus field inside the channel, due to which, spin precession occurs and spin-current reduces. Furthermore, there occur various spin relaxations inside the channel of spin-FET like DP (D'yakonov Perel) relaxation, BAP (Bir-Aronov-Pikus) relaxation or EY (Elliott-Yafet) relaxation and superfine interaction which contributes to the drastic changes in spin currents in case of different channel materials [19–24].

In the case of InAs based Spin-FET, the region of NDR is wide and hence have potential applications in analog electronics, but at the same time, the magnitude of the current is very low (refer Fig. 3(a)). However, if we take the case of InP based Spin-FET, the region of NDR is not as wide as in the case of InAs, but the magnitude of current improves to a larger extent (Refer Fig. 4(a)). Similarly, in AlSb based Spin-FET, the region of NDR is narrower as compared to the InAs based Spin-FET and InP based Spin-FET, but the magnitude of current is high, and hence, the problems of current drive cannot be faced in the Spin-FET with AlSb as channel material. Since InAs and InP are direct bandgap semiconductors, while AlSb is an indirect bandgap semiconductor, the effect of which can be observed from the ripples produced in IV curves, viz., less in InAs and InP while more in AlSb based Spin-FETs. The table for peak to valley current ratio (PVCR) is given in Table 1. From Table 1, it is clear that PVCR is maximum for GAA Spin-FET having AlSb channel material and minimum for InAs based GAA Spin-FET.

TABLE 1. Calculated PVCR of different channel material based GAA-SFETs

	I (for InAs Spin-FET)	I (for InP Spin-FET)	I (for AlSb Spin-FET)
PVCR	9	30	40

4. Conclusions

In this study, the transport properties of proposed gate all-around spin field effect transistors were studied with comparative studies. The I-V and conduction curves show that the proposed device with different channel materials can exhibit negative differential resistance (NDR). The NDR is attained in the proposed device due to the tunneling mechanism caused by the perpendicular transport in heterostructure formed by combination of materials with different bandgap. In addition, the nature of the channel material changes the I-V and conductance curves. The employed channel materials are indium arsenide (InAs), indium phosphide (InP) and aluminum antimonide (AlSb) which differs in forbidden energy gap at 300 K and also vary in structure. The simulated models therefore can find massive uses in analog electronics and specifically in the design of oscillators. Additionally, it has the remarkable potential in designing various logic gates and digitals circuits as the size is in the nanoscale regime. Furthermore, the proposed spin-device will address the power issues, which is the main concern in the contemporary world, and at the same time can work in nanoscale-regime, thereby offering increase in chip density, functionality and decreased power consumption.

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References

[1] Friedman J.S., Rangaraju N., Ismail Y.I. and Wessels B.W. A Spin-Diode Logic Family. *IEEE Trans. on Nanotechnology*, 2012, **11**(5), P. 1026–1032.

[2] Sun Z., Bi X., Li H., Wong W.F., and Zhu X. STT-RAM Cache Hierarchy with Multiretention MTJ Designs, *IEEE Trans. On VLSI systems*, 2014, **22**(6), P. 1281–1293.

[3] Malik G.F.A., Kharadi M.A. and Khanday F.A. Electrically Reconfigurable Logic Design Using Multi-Gate Spin Field Effect Transistors. *Microelectronics Journal*, 2019, **90**, P. 278–284.

[4] Malik G.F.A, Kharadi M.A., Parveen N. and Khanday F.A. Modelling for Triple Gate Spin-FET and Design of Triple Gate Spin-FET-Based Binary Adder. *IET Circuits, Devices and Systems*, 2020, DOI: 10.1049/iet-cds.2019.0329.

[5] Datta S. and Das B. Electronic analog of the electro-optic modulator. *Appl. Phys. Lett*, 1990, **56**(7), P. 665467.

[6] Sugahara S. Spin MOSFETs as a basis for integrated spin-electronics, Proceedings of 2005 5th IEEE Conference on Nanotechnology, Nagoya, Japan, 2005, P. 1243–1279.
[7] Sato Y., Gozu S., Kita T. and Yamada S. Study for realization of spin-polarized field effect transistor in $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ heterostructure. *PHYSICA E*, 2002, **12**(4), P. 399–402.
[8] Pramanik S., Bandyopadhyay S. and Cahay M. Spin transport in nanowires. *Third IEEE Conference on Nanotechnology*, IEEE-NANO, Virginia, 2003, **2**, P. 87–90.
[9] Nitta J. and Bergsten T. Electrical Manipulation of Spin Precession in an InGaAs-Based 2DEG Due to the Rashba Spin-Orbit Interaction. *IEEE Trans. on Electron devices*, 2007, **54**(5), P. 955–960.
[10] Takahashi S. and Maekawa S. Spin injection and detection in magnetic nanostructures. *Phys Rev B*, 2003, **67**(5), P. 52409.
[11] Chen X. and Tan C.M. Modeling and analysis of gate-all-around silicon nanowire FET. *Microelectronics Reliability*, 2014, **54**(7), P. 1103–1108.
[12] Shah K.A. and Parvaiz M.S. Negative differential resistance in BN co-doped coaxial carbon nanotube field effect transistor. *Superlattices and Microstructures*, 2012, **19**(2), P. 299–303.
[13] Sai M.A., Mei L.I., Xin Z.Y. and Peng Z. Negative differential resistance in a molecular junction of carbon nanotube and benzene. *SCIENCE CHINA Physics, Mechanics and Astronomy*, 2011, **54**(8), P. 1433–1437.
[14] Grassi R., Gnudi A., Lecce V.D., Gnani E., Reggiani S. and Baccarani G. Exploiting negative differential resistance in monolayer graphene FETs for high voltage gains. *IEEE Trans. on Electron Devices*, 2014, **61**(2), P. 617–624.
[15] Sengupta A. and Mahapatra S. Negative differential resistance and effect of defects and deformations in MoS2 armchair nanoribbon MOSFET. *Journal of Applied Physics*, 2013, **114**(19), P. 194513(1-5).
[16] Wu Y., Farmer D.B., Zhu W., Han S.J., Dimitrakopoulos C.D., Bol A.A., Avouris P. and Lin Y.M. Three-Terminal Graphene Negative Differential Resistance Devices. *American Chemical Society*, 2012, **6**(3), P. 2610–2616.
[17] Kharadi M.A., Malik G.F.A, Shah K.A. and Khanday F.A. Sub-10-nm Silicene Nanoribbon Field Effect Transistor. *IEEE T Electron Dev.*, 2019, **66**(11), P. 4976–4981.
[18] Atomistic Tool Kit version 13.8.1 currently available online at www.quantumwise.com.
[19] Santos T., Lee J., Migdal P., Lekshmi I., Satpati B. and Moodera J. Room temperature tunnel magnetoresistance and spin polarized tunneling through an organic semiconductor barrier. *Phys. Rev. Lett.*, 2007, **98**, P. 016601.
[20] Yue G., Chen L., Barreda J., Bevara V., Hu L., Wu L., Wang Z., Andrei P., Bertaina S. and Chiorescu I. Sensitive spin detection using an on-chip SQUID-waveguide resonator. *Appl. Phys. Lett.*, 2017, **111**(20), P. 202601.
[21] Jedema F.J., Nijboer M.S., Philip A.T. and Wees B.J.V. Spin injection and spin 26 accumulation in all metal spin valves. *Phys. Rev. B*, 2003, **67**, P. 085319.
[22] Pramanik S., Bandyopadhyay S. and Cahay M. Spin relaxation of "upstream" electrons in quantum wires: Failure of the drift diffusion model. *Phys. Rev. B*, 2006, **73**, P. 125309.
[23] Merkulov I.A., Efros A.L. and Rosen M. Electron spin relaxation by nuclei in semiconductor quantum dots. *Phys. Rev. B*, 2002, **65**, P. 205309.
[24] Amasha S., MacLean K., Radu I., Zumbuhl D.M., Kastner M.A., Hanson M.P. and Gossard A.C. Electrical control of spin relaxation in a quantum dot. *Phys Rev Lett.*, 2008, **100**(4), P. 046803.