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1-bit and 2-bit comparator designs and analysis for quantum-dot cellular automata

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In PCs, the number of arithmetic operations, the comparator is a vital equipment unit, consisting of complementary metal-oxide-semiconductor (CMOS) technology. Another procedure, referred to as Quantum Cellular Automata (QCA) will supplant the CMOS outlines, having leverage concerning zone, control utilization, and latency. The primary QCA circuits planned with the inverter and majority voter entryways. In this paper, we utilize the clocking method 180 out of phase clock crossover to outline the 1-bit comparator and compare with the current outcomes. The new proposed wire crossing plan lessens the quantity of cells required to configuration, power and area necessities. Additionally, we planned 2-bit comparator having 11 majority gates (voters), 2 number of crossovers with 0.38 μm^2 area, 203 number of cells. The designed 1-bit comparator contrast and the past outcomes where cells, region, delay demonstrates 53.57 %, 50 % and 33.32 % improvement respectively.

Keywords: QCA design, wire crossing, comparator, Ex OR gate.

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1. Introduction

A few advanced microchips that have been popularized in the 21-st century incorporate decimal number juggling equipment units. This is a reaction to procuring requests for sophisticated calculations which are necessary for cost-saving and mechanical applications. As the preparing requests approach galactic measurements, the PC business is considering the possible development towards new rising advancements to defeat CMOS limitations for execution speed and wide power scattering on limiting the incorporated circuits [1–4].

The present crucial breaking points in CMOS circuit's calculations and development of quantum mechanical impacts in exponentially as of recently added quantum circuits to another dimensional tending of the electronic group [5, 6]. As a consequence, quantum calculation and data remain an appealing territory of research over the most recent few decades [7]. This shows that superior information of quantum mechanics is required.

The innovation of quantum dot cell automata (QCA) proposed by Lent and Tougaw, is plainly becoming one of the developing advances without bounds PCs due to its minor component sizes, ultra-low power utilization, straightforward conceptualization [8, 9].

Quantum dot cellular automata are the processing with cell automata confined with varieties of quantum dots. A QCA cell is a Nano shell device ready to encode data by two electron shape. Current advancement of quantum computing continues from numerous viewpoints; quantum circuit's combination is the massive test in the quantum information handling and the improvement of the quantum PC engineering [10].

2. Quantum DOT Cellular Automata (QCA)

2.1. Background: How QCA charge transfer?

A QCA cell can be seen as an arrangement of four charge vessels or "specks", set in the corners of a square. The cell is pick up accuse of two free electrons which are able to burrow between dots. QCA are exhibited coulomb coupled quantum dot cells. Electrons situated in every cell have characteristic states with characteristic relate charge scattering. The condition of every cell is checked by its significant interaction with adjoining cells [26]. Bury cell barriers entirely repress charge exchange between the cells. The limit condition of last cells which go about as an information and yield cells which rely upon numerous electron frameworks in the composed circuit. Edge cells are controlled by the communication of electrostatic charge. With the computational issue settled one can outline the QCA design of the cells change starting from the earliest stage of electrons to arrangement state. We have watched the electron move in the wire (course of action of cells by adjoining) to perform general calculations.

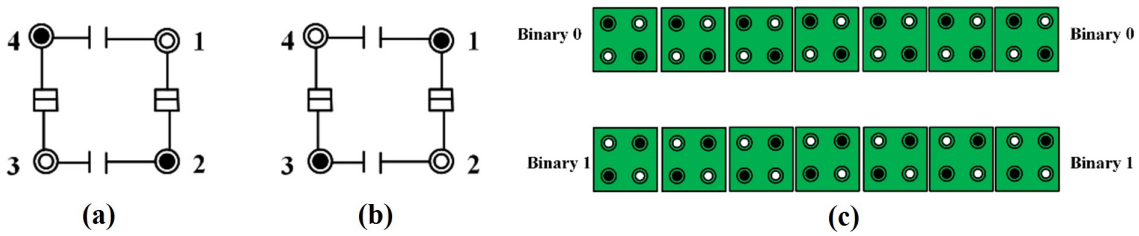


FIG. 1. (a) (b) QCA cell negative polarization denoted as logic "0"; (b) QCA cell with positive polarization denoted as "1"; (c) QCA wire showing charge transfer

A regular illustration of a solitary QCA cell is shown in Fig. 1(a,b). This figure demonstrates that a cell of four quantum dots organized in a square. There are two electrons inside the cell and passage obstructions between adjoining destinations [11, 12]. Burrowing out of the cell is thought to be totally stifled. QCA cell measure was reduced to nuclear measurements. As cell measure diminished the energy part between stationary states increments and the fleeting reaction turns out to be speedier. The close neighbor separation between dots inside a standard cell is 20 nm, the burrowing energy between dots is 0.3 meV.

2.2. Clocking

The timing of QCA, follow the semi adiabatic timing system. This system consists of four stages: switch, hold, release (discharge) and relax (unwind). At first, when the potential energy of the electron is low and the electron isn't equipped for burrowing between quantum dots, it has a definite extremity. With the start of the switch stage, the potential vitality of electrons begins to rise and toward the finish of this stage the electron achieves its most extreme potential vitality. Amid the hold stage the electron keeps up its greatest potential energy and turns out to be totally delocalized losing its polarity. In the discharge stage the potential energy of the electron begins to decrease and the cell moves incrementally towards a definite polarity. Amid the last stage i.e. the unwind stage the electron keeps up least energy and is excessively powerless, making it impossible to burrow between the dots. Along these lines, the cell achieves a definite extremity. Each QCA engineering involves four clock zones, if not less, each of which contains the above said four clock stages. Each check zone is out of stage with the following check zone as appeared in Fig. 2(a). The different check zones in a QCA design are spoken to by different hues. The shading codes we have utilized is appeared in Fig. 2(b).

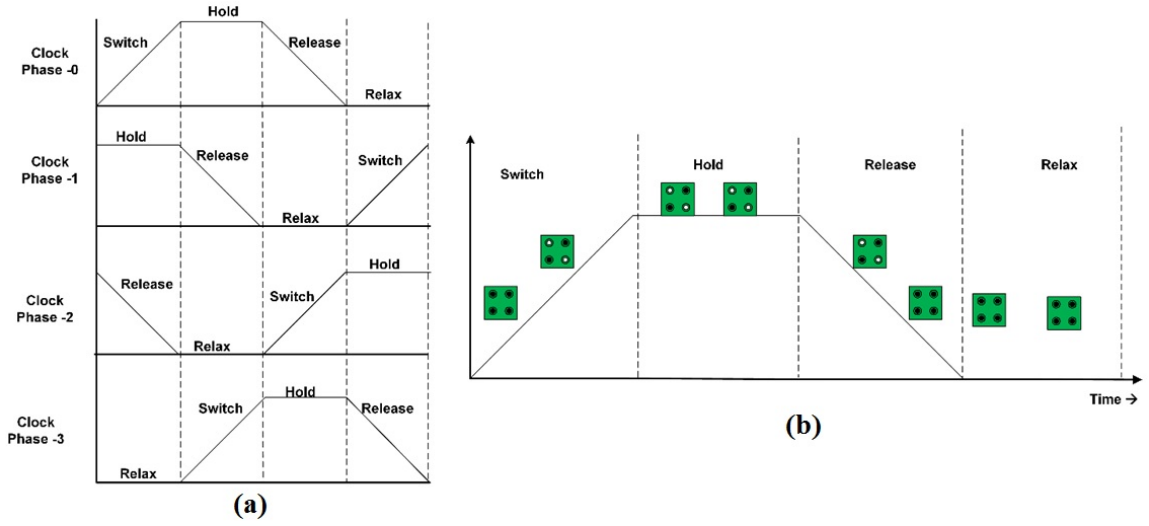


FIG. 2. (a) QCA cell with clocking; (b) Propagating of QCA cell in clock zones

The principle contrast between CMOS configuration circuits and QCA configuration circuits is that in the CMOS, the clock flag controls the circuit yield and states, whereas in QCA, the clock is valuable to exchange the charge information from one cell to next contiguous associated cell. On each clock cycle every cell discharge or evacuates its state and each cell in QCA including info and yield cells are clock controlled [13].

2.3. Wire crossing technique

For efficient design of QCA circuit in a smaller footprint, one area of primary consideration is wire crossing. Wire crossing is vital in QCA based plan and numerous strategies have been proposed to outline an efficient wire crossing, for example, coplanar based and the multilayer based methods, recently. Meanwhile the wire crossing strategies utilizing the control of clock stage have also been proposed [14]. Keeping in mind the end goal to outline the wire crossing using the said procedures, extra undertakings ought to be requested, for example, interpretation or rotation of QCA cells control of clock stage, expansion of bigger and soon. Like this their methods require extra time or spatial intricacy.

i) Coplanar based wire crossing procedure was proposed by Tougaw and Lent is shown in Fig. 3(a) basic geometry of the coplanar based wire crossing system [18, 19]. In this illustration the vertical wire and even wires are transmitting the values of 1 and 0 separately. To actualize this wire crossing the cell of horizontal wire are rotated by 45 °. On the off chance that the length of the vertical wire after a crossing point cell is adequate a transmitting value is not influenced by the other wire [14]. Likewise the horizontal wire should consist of an odd number cells, since the property of the rotated cells has an inverter chain that the polarization substitutes heading between neighboring cells. Cells rotated by 45 ° initiate the extra space between cells. It inherently diminishes the energy partition between the ground state and the primary energized state which debases the execution of such a device as far as highest working temperature, protection from entropy, and least exchanging time [15].

ii) Multilayer-based wire-crossing strategy utilizes a hybrid crossover technique. This approach is similar to that of the coplanar-based method from the perspective of the floor design since it would seem that appearance of two wires crossing. Truth be told, it comprises of the stereoscopic structure. In spite of the fact that this strategy has a few focal points, the noise issue between convergence cells in the hybrid territory is present [6]. There are additionally a few things to consider for plan and recreation forms in QCA Designer, for example, the quantity of layers, crossover and vertical cells [16].

iii) QCA wire crossing is utilizing the different of clock system we consider the idea of QCA clock stage, for instance the information of present clock region is obtained from the past clock region. In this new technique each non-neighboring clock area does not influence the inverse clock area. In this plan wire crossing depends on the distinction of 180 ° between two nonadjacent clock regions. However in this strategy a bit much of 45 ° rotation of cells utilized as a part of co planar wire intersection and sub layers courses of action as utilized as a part of multi-layer wire crossing technique the nitty gritty wire crossing information appeared in Fig. 3(b) utilizes an inverse stage wire clock 0 and clock 2 and in Fig. 3(c) utilizes clock 1 and clock 3 wires used to information stream, the convergence cell can be have a place with any of two wires (either clock 0 or clock 2 in Fig. 3(b) and clock 1 or clock 3 in Fig. 3(c)) and there is no interface with each other.

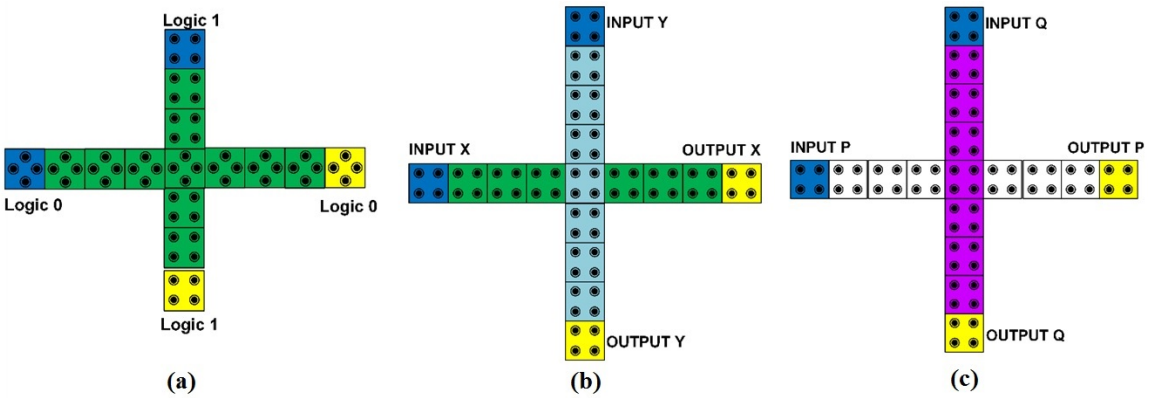
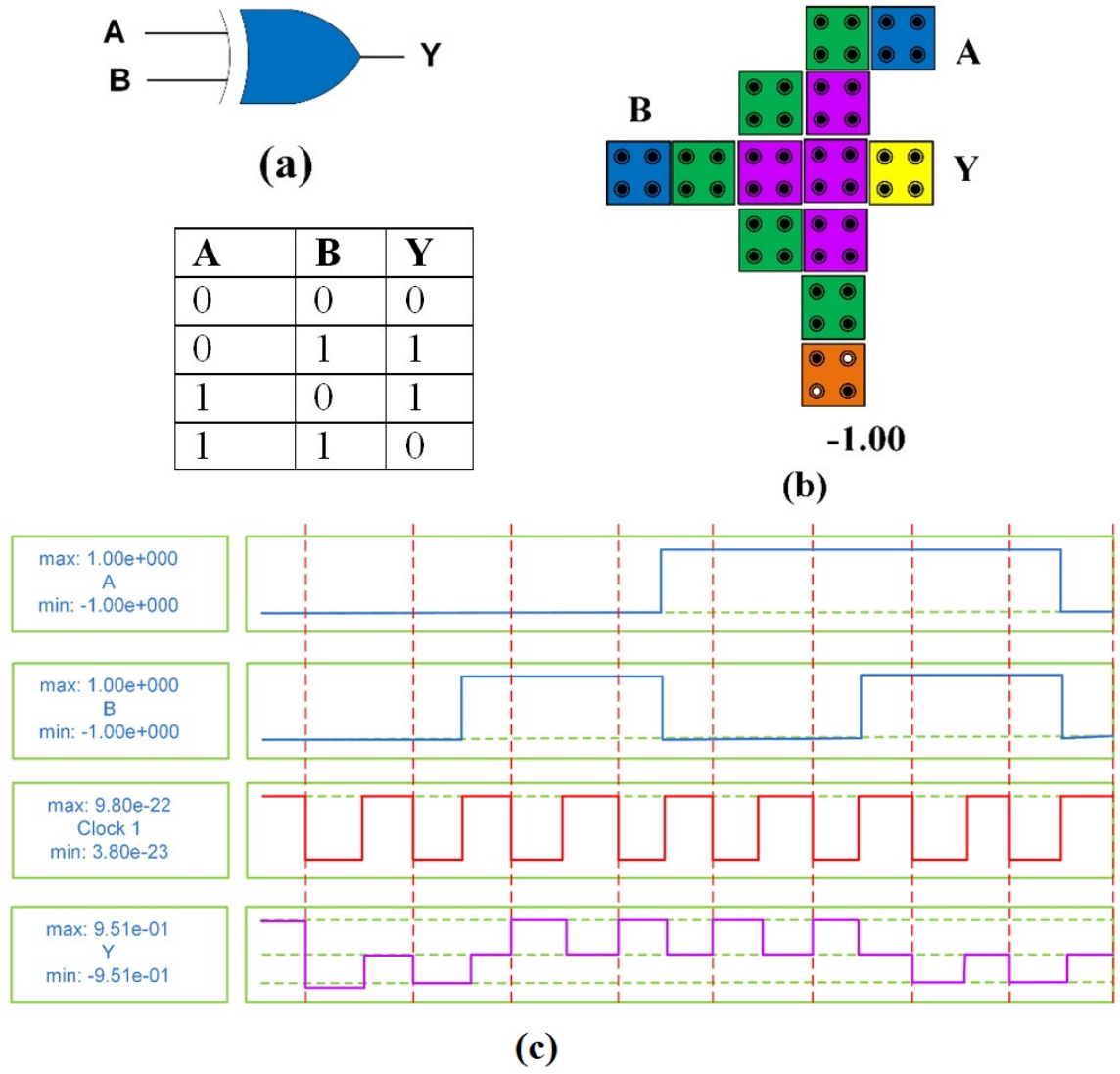


FIG. 3. (a) Co Planar wire crossing; (b) wire crossing using clock 0 and clock 2; (c) wire crossing using clock 1 and clock 3

3. Exclusive OR gate QCA layout

To outline any computerized rationale circuits fundamental entryways AND,OR, NOT and NAND,NOR universal gates are utilized. Notwithstanding that EX-OR additionally utilized for outline of complex circuits like adders, comparators and multipliers so on [17–19].

Here we demonstrated the new format engineering of EX-OR entryway consisting of 13 cells with $1/2$ clock delay (Fig. 4). In Table 1, the examination of given EX-OR entryway is demonstrated. This composed EX-OR gate extremely helpful to limit the QCA facilitate format regarding number of cell and clock delay.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

FIG. 4. (a) EX-OR gate symbol and truth table (b) QCA layout Design for a EX-OR gate (c) Simulation waveform

TABLE 1. QCA Ex-OR gate layout comparison analysis

XOR gate in	Area (μm^2)	Delay Clock Cycles	Majority gates count	Number of cells
[20]	0.06	1.25	3	67
[21]	0.02	1	3	32
[22]	0.0233	0.75	4	30
[23]	0.02	0.75	4	28
proposed design	0.01	0.5	1	13

4. Simulation results and discussion

The essential function of a comparator is to regard the magnitude of two binary data to determine their relationship. The EX-NOR gate can be utilized as a fundamental comparator in light of the fact that its output is a 1. On the off chance that the two information bits are equivalent and a 0 if the information bits are not equivalent. we demonstrated 1 bit and 2 bit comparator composed utilizing QCADesign programming with wire crossing uses an inverse clock (180 phase shift) system and actualized with most recent EX-OR entryway. Fig. 5(a,b) demonstrates the 1 bit and 2 bit comparator and planned with fewest number of logic gates. The logic concerns the yield of two bits (A, B) less than ($W1$, $W2$), equal ($X1$, $X2$), or greater than ($Y1$, $Y2$) of 1 bit and 2 bit comparator spoke to with logic condition appeared underneath after streamlined with the K-map.

The logic for a 1 bit comparator outputs is as follows:

$$W1 = A'B, \tag{1}$$

$$X1 = AB + A'B' = A \odot B, \tag{2}$$

$$Y1 = AB'. \tag{3}$$

The logic for a 2 bit comparator outputs is as follows:

$$W2 = A1'A0'B0 + A1'B1 + A0'B1B0 = A1'B1 + (A1 \odot B1)A0'B0, \tag{4}$$

$$X2 = A1'B0'B1'B0' + A1'A0B1'B0 + A1A0B1B0 + A1A0'B1'B0' = (A1 \odot B1)(A0 \odot B0), \tag{5}$$

$$Y2 = A1A0B0' + A1B1' + A0B1'B0' = A1B1' + (A1 \odot B1)A0B0'. \tag{6}$$

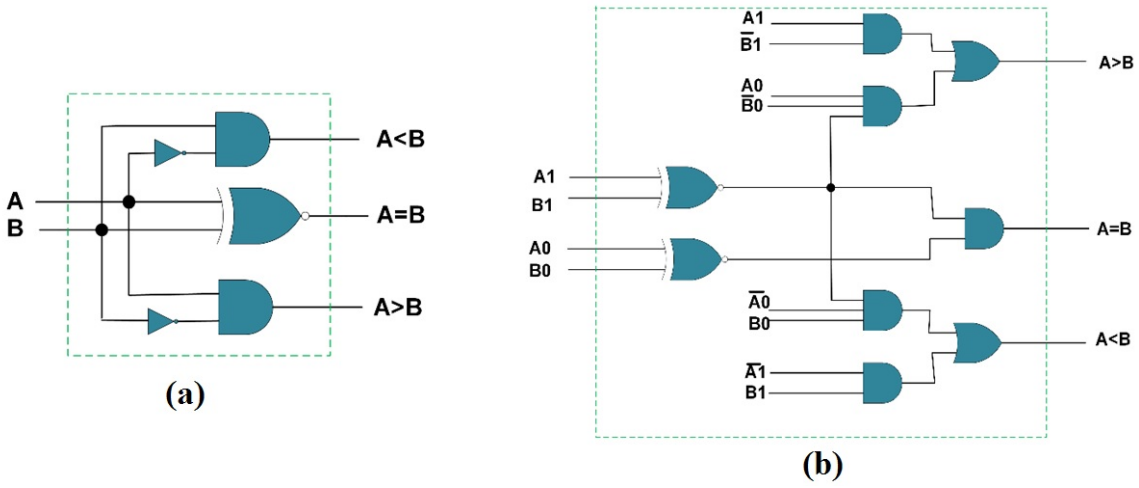


FIG. 5. (a) 1 bit comparator logic circuit; (b) 2 bit comparator logic circuit

TABLE 2. QCA layout analysis of proposed comparators

Name of the comparator		Area (μm^2)	Delay in Clock Cycles	Number of Clock Phases	Number of cells	Wire crossing
1 bit comparator	[24]	0.343	4	16	319	Co-planar
	[25]	0.182	1	4	117	Co-planar
	[26]	0.127	1.25	5	100	Co-planar
	[27]	0.103	1.25	5	95	Multilayer
	Proposed	0.10	0.5	2	60	180 ° clock phase shift
2 bit comparator	Proposed	0.38	1.25	5	203	180 ° clock phase shift

Figure 6(a,b) demonstrates 1 bit comparator and 2 bit comparator planned with no extra assignments, in those outlines we are disposed to utilize consistent coplanar or multilayer wire crossing; here composed circuits utilized 180 clock phase shift wire crossing. Fig. 7 demonstrates the results were obtained with high polarization and less noise. It is regular to assess any QCA circuit as far as the area utilized, clock delay and a number of cells utilized.

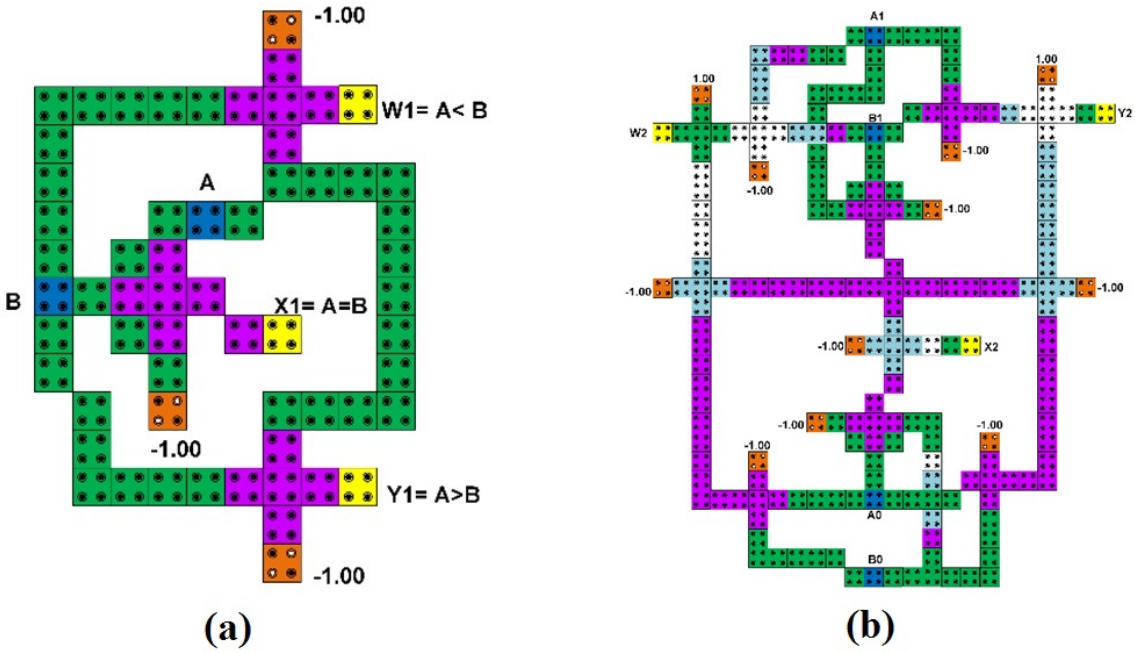


FIG. 6. (a) Proposed 1 bit comparator QCA layout; (b) Proposed 2 bit comparator QCA layout

It has been noted that our designs utilize fewer cells and has less delay. In Table 2, one can see the correlation of past plans and furthermore recorded the proposed 2 bit comparator not compared and the past outlines in light of its inaccessibility in the current literature.

5. Conclusions

The more significant part of QCA combinational circuits with coplanar or multilayer wire crossing it have many-sided outline quality is more. In this paper we proposed a smaller comparator with clock 180 degree wire crossing technique. We composed this QCA design in the QCADesign test system. The proposed 1 bit comparator layout cell count less than 36.84 % of most recent outline and area occupation are less than 2.91 % with delay utilizes just $1/2$ clock, whereas the 2 bit comparator possesses range 0.38 μm^2, cell count 203 with clock delay of $1\ 1/2$.

Generally, QCA circuits have incredibly noteworthy wiring delays for a quick plan in QCA, many-sided quality imperatives are exceptionally basic issues and the outline needs to utilize compositional systems to support the speed considering these limitations. The QCA innovations once realized will probably require a change in the outline rules. These outlines utilized the given particular plan rules, however as in a CMOS plan they can be scaled in a similar manner. This provides a chance to contrast the abnormal state outline engineering and in QCA circuits.

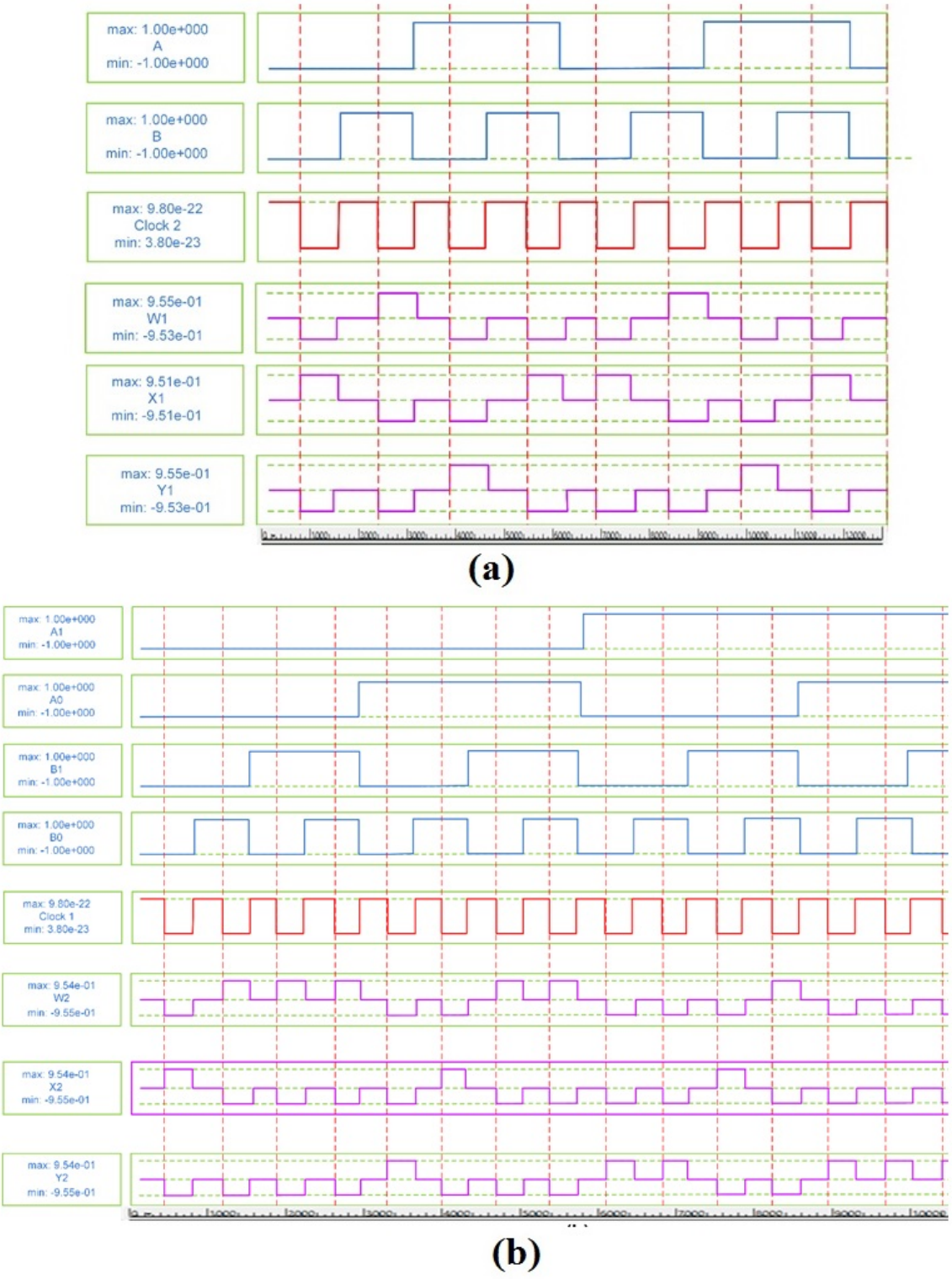


FIG. 7. Simulation results of proposed comparators: (a) 1-bit comparator; (b) 2-bit comparator

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