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A new efficient non-reversible 4 bit binary to gray and 4 bit gray to binary converter in QCA

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The present Very Large Scale Integration (VLSI) technology is based on Complementary Metal-oxide-Semiconductor (CMOS) technology. The development of the VLSI technology has reached its peak due to the fundamental physical limits of CMOS technology. The recent challenges, as well as the physical limitation of the traditional CMOS technology, has overcome by the Quantum-dot Cellular Automata (QCA) which is first introduced by C. S. Lent. The nanoscale size quantum cell is a feature of QCA technology. In this paper, we propose a new QCA structure for 4-bit binary to 4-bit gray and 4-bit gray to 4-bit binary using two input XOR gate. These structures are designed and simulated with QCA designer and compared with previous structure.

Keywords: quantum-dot cellular automata (QCA), binary code, gray code, converter, QCA cell, QCA designer.

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1. Introduction

Quantum Dot Cellular Automata (QCA) is one of the new and fledgling technology at the nanoscale [1] has been used widely in digital circuits and systems, also an innovative access towards the present age of nanotechnology, a substitution of contemporary CMOS technology [2] and proposes a novel designing technique which is appropriate for logic circuits. Presently, CMOS technology has faced many problems such as delay, power consumption, size of circuits, the area [1, 3–5], deteriorating supply voltage, power dissipation; hinder the microelectronics momentum using regular circuit scaling [1]. By using this technology, these problems are generated and different new technologies have recently been proposed to overcome these problems [6, 7]; QCA is one of them. Electron transformation in IC technology is known as current flow in the device, but in QCA. there is no current flow only charge transformation, which is why this technology requires exceedingly low power for computing. Logic state representation is the main characteristic of this technology, not in terms of voltage levels but alternately represented in terms of logic cells. In QCA, coulombic interaction is caused to create the necessary computing logic states of 1 and 0; this technology uses less device to perform the calculation. This computing of logical states is created by the position of the electrons inside the QCA cells. These cells are the group of basic parts. QCA logic gates and circuits are carried out by these cells. In QCA, these cells have been replaced in lieu of hardware components [8]. In recent years, several QCA based logic circuits have been proposed [9–16].

2. Quantum DOT Cellular Automata (QCA)

2.1. Basic QCA gate

A basic QCA cell comprises four quantum dots in a square shape coupled with tunnel barriers. To represent the information, quantum dot cellular automata use a binary logic. In a QCA logic device, two types of arrangements are normally seen denoted as cell polarization; $P = +1$ and $P = -1$, which represent "1" and "0" respectively are shown in Fig. 1. Through the charge configuration of the QCA cell, binary information is encoded. In any traditional logic circuit, data is exchanged by the electrical current but QCA works by the Columbic communication that associates the condition of one cell to the condition of its neighbors, which results in data change. All cell in a line with same polarization is known as QCA wire, shown in Fig. 2.

In QCA, majority voter gate and inverter act as the basic gate. The majority voter (MV) gate generates an output 1 if the majority of inputs are 1, as shown in Fig. 3(a). The logical operation of majority voter gate is shown in eq. (1):

$$\mathrm{MV(A, B, C)} = \mathrm{AB} + \mathrm{BC} + \mathrm{AC}. \tag{1}$$

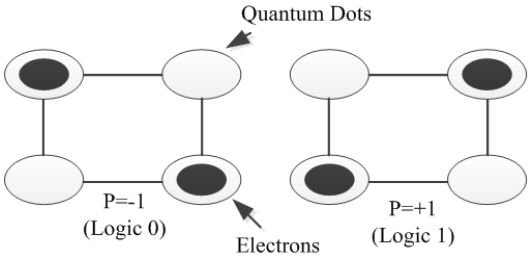


FIG. 1. Two different polarization

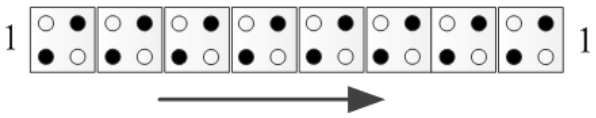


FIG. 2. QCA wire

We can implement the AND gate and OR gate from the majority voter by fixing the input (control input) permanently to a 0 or 1. The logical operation of AND gate and OR gate from the majority voter gate is shown in eq. (2) and eq. (3) respectively. If the control input is permanently set to 1, then it will work as an AND gate, shown in Fig. 3(b). Similarly, if the control input is 0 then it is an OR gate is shown in Fig. 3(c).

$$\mathrm{MV(A, B, 1) = A + B}, \tag{2}$$

$$\mathrm{MV(A, B, 0) = AB}. \tag{3}$$

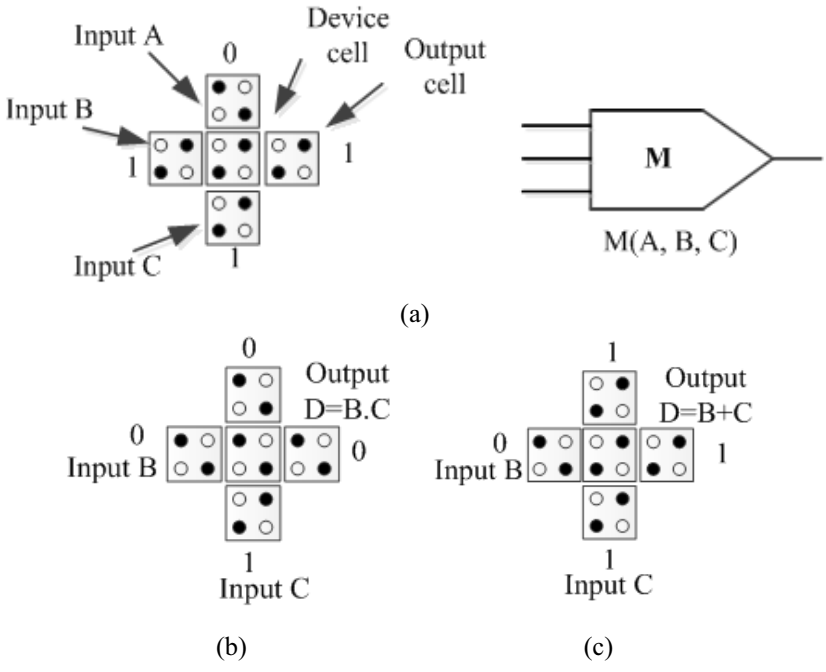


FIG. 3. (a) Majority voter gate; (b) AND gate; (c) OR gate

2.2. XOR gate

Quantum Logical Circuit has several logical gates, among which XOR Gate is one [17,18]. XOR gate is used in many circuits, so it is very important. There are several structures for this gate, one of which is shown in Fig. 5.

The basic operation of XOR gate is $(A \operatorname{xor} B)$ or $F(A, B) = A\overline{B} + \overline{A}B$. The above structure can be implemented as QCA design shown in Fig. 6(a). The result of simulation of this design is shown in Fig. 6(b).

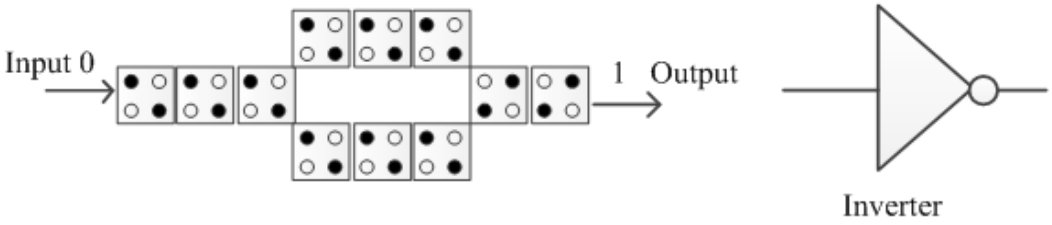


FIG. 4. Inverter

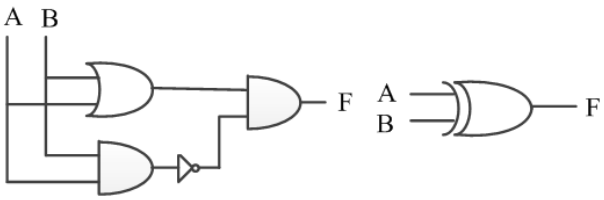


FIG. 5. Schematic of XOR gate

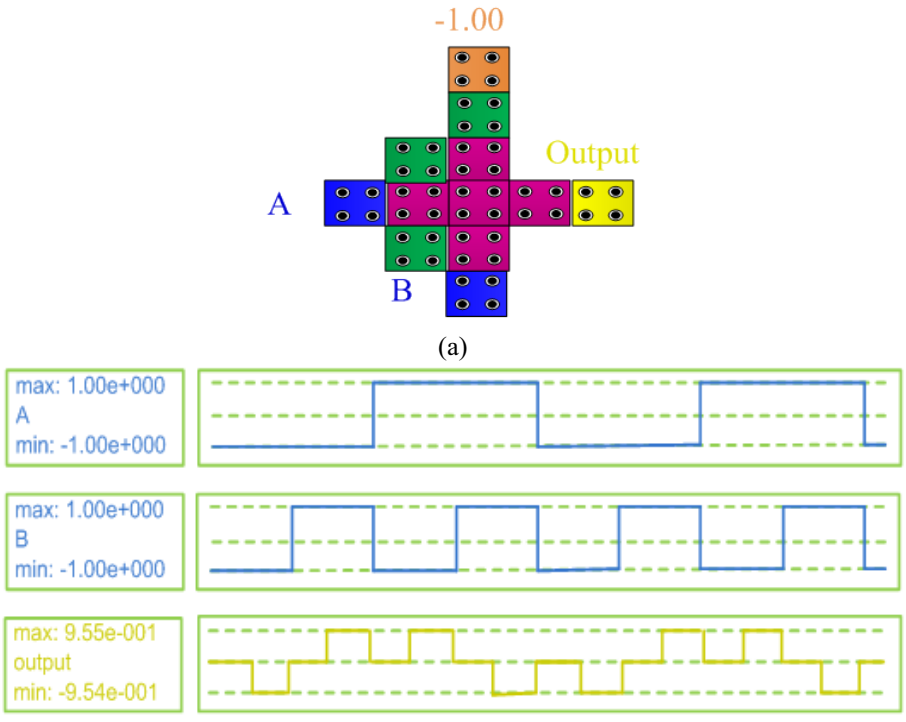


FIG. 6. XOR gate: (a) QCA layout; (b) Simulation result

3. Non-reversible 4-bit binary to 4-bit gray code converter

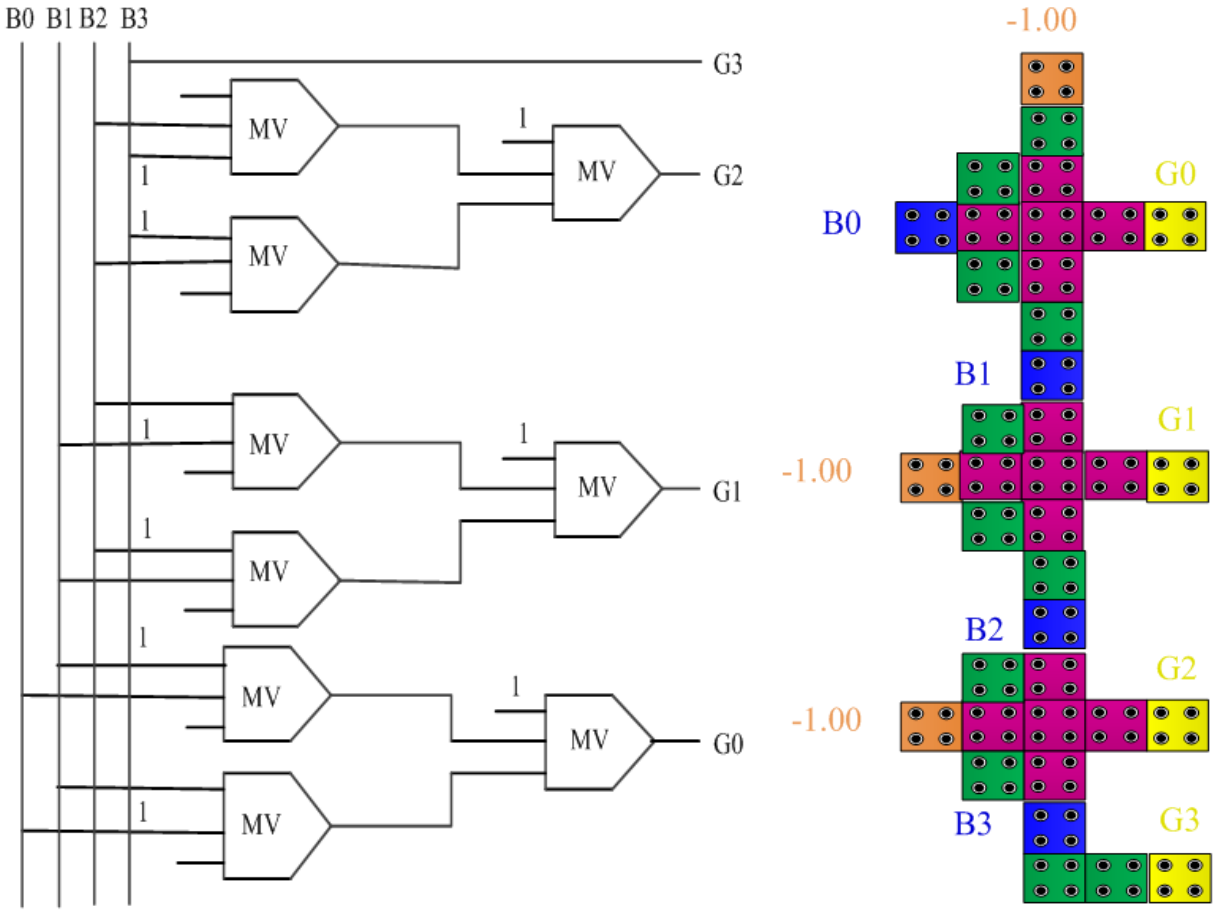
A circuit is said to be non-reversible if it does not contain an equal number of inputs and an equal number of outputs. On the other hand, the non-reversible circuit is a circuit whose inputs cannot be reconstructed from its outputs.

The simplest form of computer code or programming data is called Binary code which is represented entirely by a binary system of digits consisting of a string of consecutive zeros and ones. In binary to gray code conversion, the Most Significant Bit (MSB) of the gray code is always equal to the MSB of the given binary code and by doing XOR operation between binary code bit at that index and previous index, the other bits of the output gray code can be obtained.

In this section, we have proposed the non-reversible 4-bit binary to 4-bit gray code converter structure using two-input XOR gate. For non-reversible 4-bit binary to 4-bit gray code converter, inputs are described as B0, B1, B2, and B3 where corresponding outputs are G0, G1, G2, and G3. It is observed that three two-input XOR gates are needed to design non-reversible 4-bit binary to 4-bit gray code converter. The first XOR gate generates G0 and XOR of B0, B1. The second XOR gate generates G1 and XOR of B1, B2, while the third XOR gate generates G2 and XOR of B2, B3. The output G3 is calculated directly from input B3, so G3 = B3. Here, the polarization is set to -1 which is used as fixed polarization. Gray code outputs equation has shown in eq. (4):

$$\mathrm{G0} = \mathrm{B0} \oplus \mathrm{B1}, \quad \mathrm{G1} = \mathrm{B1} \oplus \mathrm{B2}, \quad \mathrm{G2} = \mathrm{B2} \oplus \mathrm{B3}, \quad \mathrm{G3} = \mathrm{B3}. \tag{4}$$

In Fig. 7(a), we have shown the logical circuit of this converter as well as QCA design of this structure in Fig. 7(b). A truth table of this converter has shown on Table 2. The outcomes of the simulation of this converter have shown in Fig. 8.



(a) (b)

FIG. 7. Non-reversible 4-bit binary to 4-bit gray code converter: (a) Logical circuit; (b) QCA layout

For the proposed structure of non-reversible 4-bit binary to 4-bit gray code converter, the simulation factors values are shown in Table 3. The proposed work compared to previous works has a good improvement, especially in cell numbers and occupied areas. By comparing the previous works in [19] and [20], our proposed circuit has 37 cells which have improved 70.87 % and 80.73 %. Besides comparing the previous works in [19–22], the occupied area 90.24 %, 88.24 %, 55.56 % and 77.78 % have been reduced. The work is better than [19] because our proposed structure has no crossover. In our work, the clock cycle latency is 0.50 which is better than [19] and [20].

TABLE 1. Design factors for XOR gate

Design factor	Value
Cell count	12
Area	0.02 μm^2
Crossover	Zero
Latency	0.50

TABLE 2. Truth table of 4-bit binary to 4-bit gray code converter

Input				Output			
B0	B1	B2	B3	G0	G1	G2	G3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	1	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	1	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

TABLE 3. Simulation factor for non-reversible 4-bit binary to 4-bit gray code converter

Design factor	Proposed work	Previous work in [19]	Previous work in [20]	Previous work in [21]	Previous work in [22]
Cell count	37	127	192	105	131
Area (μm^2)	0.04	0.41	0.34	0.09	0.18
Crossover	Zero	Three	Zero	Zero	–
Latency	0.50	0.75	2	–	–

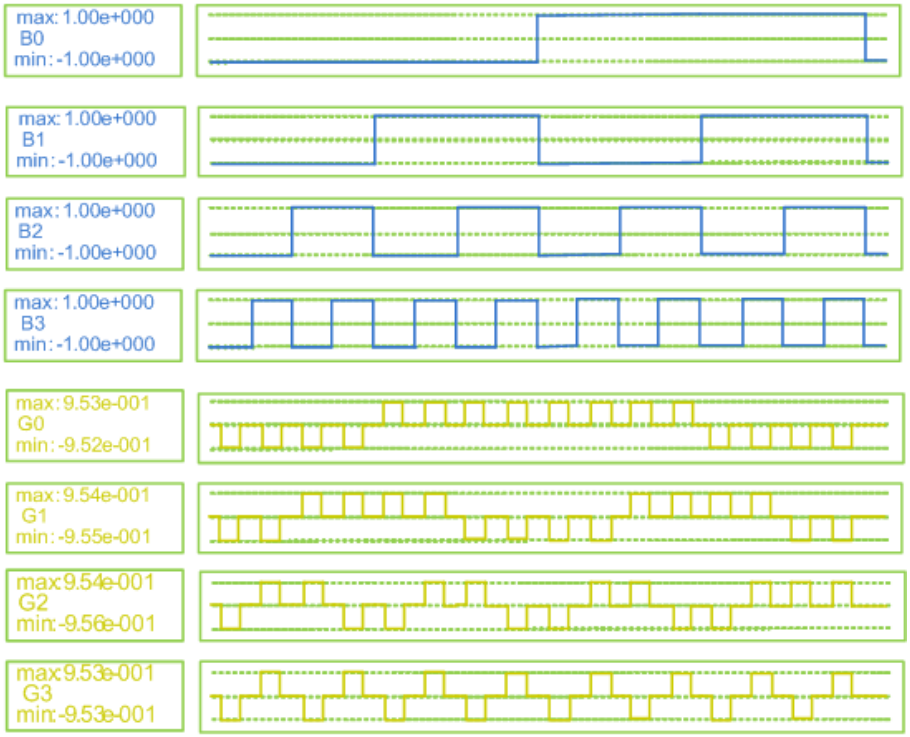


FIG. 8. Simulation result of 4-bit binary to 4-bit gray code converter

4. Non-reversible 4-bit gray to 4-bit binary code converter

Gray code is a reflected code where an ordering of $2n$ binary numbers such that only one bit changes from one entry to the next. In gray to binary code conversion, the Most Significant Bit (MSB) of the binary code is always equal to the MSB of the given binary number and by checking gray code bit at that index, other bits of the output binary code can be obtained. If current gray code bit is 0, then copy previous binary code bit. Otherwise, copy invert of previous binary code bit.

In this section, based on the XOR gate, we have also proposed a QCA circuit to convert the 4-bit gray code to 4-bit binary code. For non-reversible 4-bit gray to 4-bit binary code converter, inputs are described as G3, G2, G1 and G0 where corresponding outputs are B3, B2, B1, and B0. It is observed that three two-input XOR gates are needed to design non-reversible 4-bit binary to 4-bit gray code converter. The output B3 is calculated directly from input G3, so B3 = G3. First XOR gate generates B2 and XOR of B3, G2. Second XOR gate generates B1 and XOR of B2, G1. Third XOR gate generates B0 and XOR of B1, G0. Here, polarization is set to -1 which is used as fixed polarization. Binary code outputs equation has shown in eq. (5):

$$\mathrm{B0} = \mathrm{B1} \oplus \mathrm{G0}, \quad \mathrm{B1} = \mathrm{B2} \oplus \mathrm{G1}, \quad \mathrm{B2} = \mathrm{B3} \oplus \mathrm{G2}, \quad \mathrm{B3} = \mathrm{G3}. \tag{5}$$

In Fig. 9(a) we have shown the logical circuit of this converter as well as QCA design of this structure in Fig. 9(b). A truth table of this converter has shown on Table. 4. The outcomes of the simulation of this converter are shown in Fig. 10.

For the proposed structure of non-reversible 4-bit gray to 4-bit binary code converter the simulation factors values have shown in Table. 4. The Proposed work compared to previous works shows good improvement, especially in cell numbers and occupied areas. By comparing the previous works in [19] and [20] respectively, our proposed circuit has 47 cells which have improved 52.53 % and 82.53 %, as well as the occupied area. In our work, the clock cycle latency is 1.00 which is also better than [20].

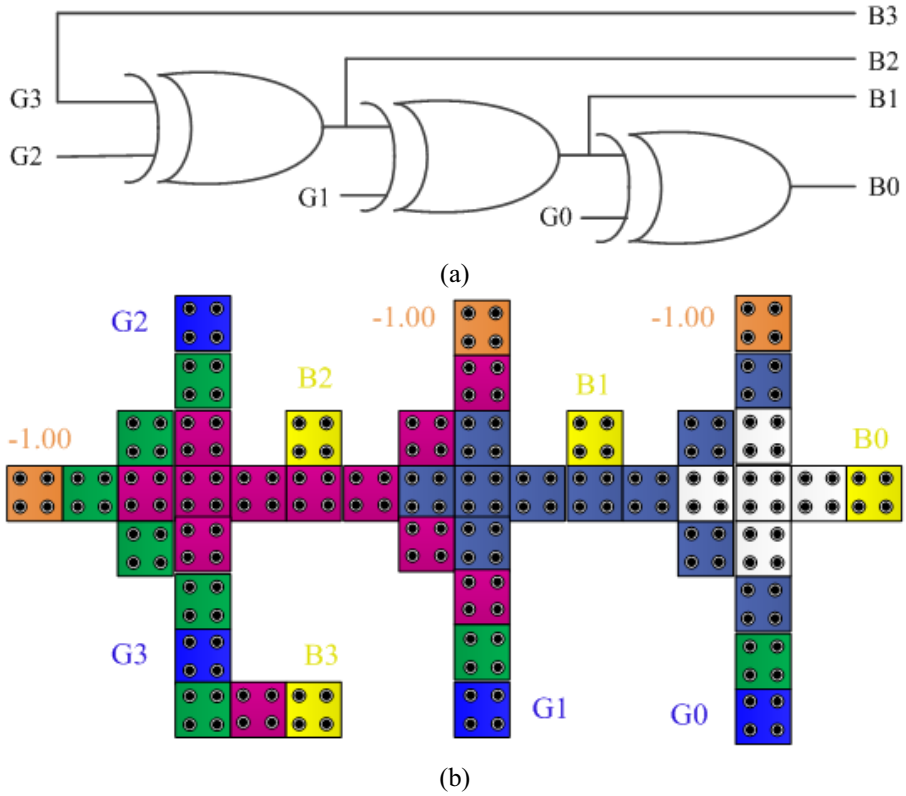


FIG. 9. Non-reversible 4-bit gray to 4-bit binary code converter: (a) Logical circuit; (b) QCA layout

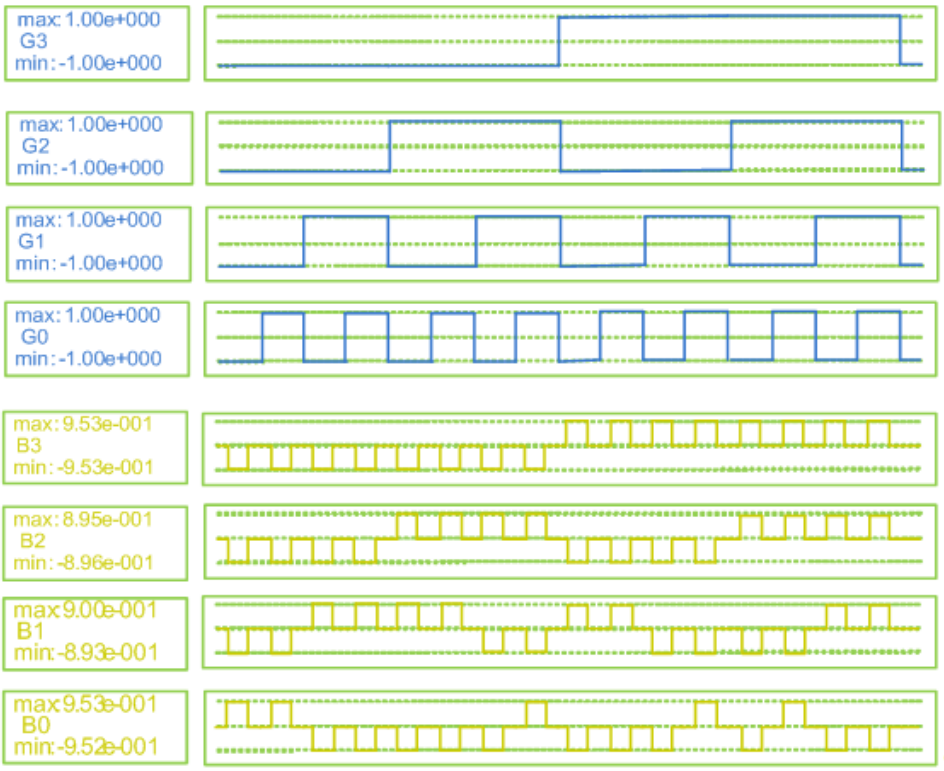


FIG. 10. Simulation result of non-reversible 4-bit gray to 4-bit binary code converter

TABLE 4. Truth table of 4-bit gray to 4-bit binary code converter

Input				Output			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

TABLE 5. Simulation factors for the non-reversible 4-bit gray code to 4-bit binary code converter

Design factor	Proposed work	Previous work in [19]	Previous work in [20]
Cell count	47	99	269
Area (μm^2)	0.05	–	0.69
Crossover	Zero	Zero	Zero
Latency	1	0.75	6

5. Power depletion of the proposed layout

The power dissipation by a QCA cell is calculated using the Hartree–Fock approximation [23–25]. The Hamiltonian matrix of a mean-field approach is illustrated as the eq. (6):

$$\mathbf{H} = \begin{bmatrix} \frac{-E_k}{2}\sum_i C_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}(C_{j-1}+C_{j+1}) & -\gamma \\ -\gamma & \frac{E_k}{2}(C_{j-1}+C_{j+1}) \end{bmatrix}. \tag{6}$$

The energy cost of two neighboring cells (i and j) with opposite polarizations is derived as follows in eq. (7):

$$E_{i,j} = \frac{1}{4\prod \epsilon_0 \epsilon_r} \sum_{n=1}^{4}\sum_{m=1}^{4} \frac{q_{i,n} q_{j,m}}{|r_{i,n} - r_{j,m}|}. \tag{7}$$

For a single QCA cell the instantaneous total power equation can be calculated as:

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}\cdot\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2. \tag{8}$$

In eq. (8), the term P_1 includes two main components: first, the power gain achieved from the difference of the input and output signal powers ($P_{in} - P_{out}$) and second, the transferred clocking power to the cell (P_{clock}) and the term P_2 represents dissipated power (P_{diss}) [24]. The upper bound power dissipation model [26] of a QCA cell can be given as eq. (9):

$$P_{diss} = \frac{E_{diss}}{T_{cc}}\frac{\hbar}{2T_{cc}}\vec{\Gamma}_+ \times \left[-\frac{\vec{\Gamma}_+}{\left|\vec{\Gamma}_+\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_+\right|}{k_BT}\right) + \frac{\vec{\Gamma}_-}{\left|\vec{\Gamma}_-\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_-\right|}{k_BT}\right)\right]. \tag{9}$$

Finally, in one clock cycle, the energy dissipation of a QCA cell is estimated as follows in eq. (10):

$$E_{diss} = \frac{\hbar}{2}\int_{-T}^{T}\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}dt = \frac{\hbar}{2}\left(\left[\vec{\Gamma}\cdot\vec{\lambda}\right]_{-T}^{T} - \int_{-T}^{T}\vec{\lambda}\cdot\frac{d\vec{\Gamma}}{dt}dt\right). \tag{10}$$

Power estimation tool known as QCAPro [25, 27–29] is used to calculate the dissipated power. Combination of leakage and switching power [24] known as the total power loss in a QCA circuit is evaluated by the QCAPro. The power dissipation map of our proposed designs is obtained at 2 K temperature with $0.5E_k$. In the following figures, high power dissipating cells are indicated using thermal hotspots with darker colors. The thermal hotspot map or power map of the proposed non-reversible 4-bit binary to gray and 4-bit gray to binary converter under energy level of $0.5E_k$ are shown in Fig. 11(a) and (b) respectively.

(a) (b)

FIG. 11. Power dissipation map for the proposed non-reversible (a) 4-bit Binary to Gray converter (b) 4-bit Gray to Binary converter at 2K temperature and tunneling energy of 0.5 E_k

In addition, the leakage, switching and total energy dissipation of proposed designs at three different tunneling energy levels ($0.5E_k$, $1.0E_k$, $1.5E_k$) at 2 K temperature is given in Table 6.

The dissipated leakage energy by the proposed non-reversible 4-bit binary to gray code converter are 12.98 meV, 35.49 meV and 60.25 meV at $\gamma = 0.5E_k$, $\gamma = 1.0E_k$ and $\gamma = 1.5E_k$ respectively and by proposed non-reversible 4-bit binary to gray code converter are 17.97 meV, 48.02 meV and 80.83 meV at $\gamma = 0.50E_k$, $\gamma = 1.0E_k$ and $\gamma = 1.5E_k$ respectively. The dissipated switching energy by the proposed non-reversible 4-bit binary to gray code converter are 27.53 meV, 23.15 meV and 19.53 meV at $\gamma = 0.50E_k$, $\gamma = 1.0E_k$ and $\gamma = 1.50E_k$ respectively and by proposed non-reversible 4-bit binary to gray code converter are 17.7 meV, 14.31 meV and 11.73 meV at $\gamma = 0.50E_k$, $\gamma = 1.0E_k$ and $\gamma = 1.50E_k$ respectively.

TABLE 6. Energy dissipation analysis of proposed non-reversible gate

Power dissipated at $T = 2$ K									
	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Total energy dissipation (meV)		
Circuit	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k
B2G Converter	12.98	5.49	0.25	7.53	3.15	9.53	0.51	8.64	9.78
G2B Converter	7.97	8.02	0.83	7.70	4.31	1.73	5.67	2.33	2.56

Finally, the total dissipated energy by the proposed non-reversible 4-bit binary to gray code converter are 40.51 meV, 58.64 meV and 79.78 meV at $\gamma = 0.50E_k$, $\gamma = 1.0E_k$ and $\gamma = 1.50E_k$ respectively and by proposed non-reversible 4-bit binary to gray code converter are 35.67 meV, 62.33 meV and 92.56 meV at $\gamma = 0.50E_k$, $\gamma = 1.0E_k$ and $\gamma = 1.50E_k$ respectively. The leakage energy, switching energy and the total energy dissipation of proposed designs are presented graphically in Fig. 12 respectively.

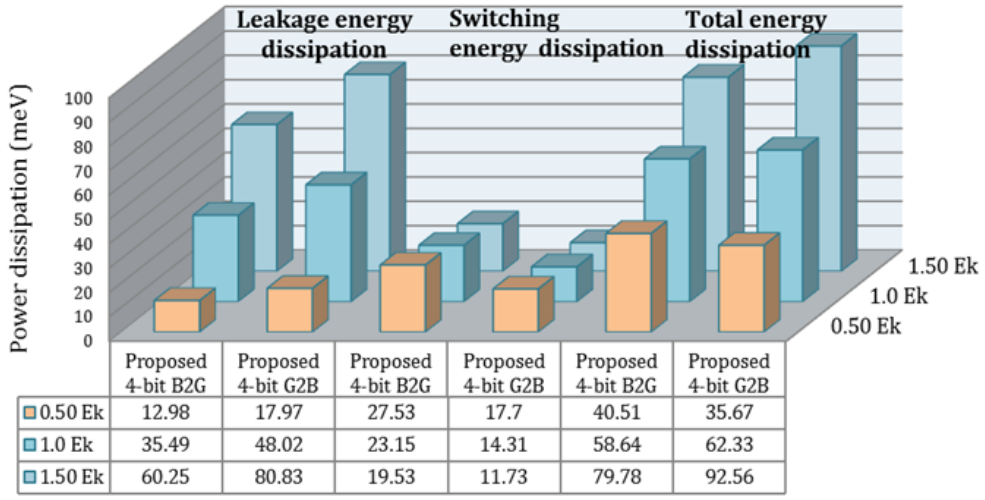


FIG. 12. Energy dissipation graph of proposed B2G and G2B at three different tunneling energy levels at temperature ($T = 2$ K)

6. Conclusion

In this paper, we have presented a 4-bit non-reversible binary to gray and vice versa converter with a new QCA design. We designed our circuits in non-reversible mode. These structures come up with improvements compared to the previous works. These proposed circuits are fit in the manner that they enclose fewer cells, clock phases, logic gate count, overall size, and area as well as distinguish them from earlier reported designs. The proposed circuits can be considered as a promising step to design highly area efficient and low power consuming complex logic circuits as well as input-output devices.

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