NANOSYSTEMS: PHYSICS, CHEMISTRY, MATHEMATICS, 2017, 8 (1), P. 75–78

Simulation of DIBL effect in junctionless SOI MOSFETs with extended gate

A. E. Atamuratov[1], M. Khalilloev[1], A. Abdikarimov[1], Z. A. Atamuratova[1],
M. Kittler[2], R. Granzner[2], F. Schwierz[2]

[1]Urganch State University, Kh. Olimjan, 14, Urganch, 220100, Uzbekistan
[2]Technical University of Ilmenau, Ehrenbergstrasse, 29, 98693 Ilmenau, Germany

atabek.atamuratov@yahoo.com, frank.schwierz@tu-ilmenau.de

PACS 85.30.Tv **DOI 10.17586/2220-8054-2017-8-1-75-78**

Short channel effects such as DIBL are compared for trigate SOI Junctionless MOSFET with extended and non-extended lateral part of the gate. A trigate SOI JLMOSFET with gate length L_{gate}, a silicon body width W_{tin} and thickness of 10 nm are simulated. In order to calculate the DIBL, the transfer characteristics of JLMOSFETs was simulated at a donor concentration of $5 \cdot 10^{19}$ cm^{-3} in the silicon body. The equivalent oxide thicknesses of the HfO_2 gate insulator used in simulation was 0.55 nm. Simulation result showed the DIBL for the trigate JLMOSFET depended on the length of the lateral part of the gate Lext. DIBL is high for devices with gates having extended lateral parts. This is a result of parasitic source (drain)-gate capacitance coupling which is higher for longer L_{ext}.

Keywords: Junctionless MOSFET, DIBL, parasitic capacitance.

Received: 8 July 2016

Revised: 30 August 2016

1. Introduction

In very short-channel MOSFET devices ($L = 10$ nm or less) the formation of ultra-sharp source and drain junctions imposes orders of magnitude of variation in doping concentration over a distance of a few nanometers. Such concentration gradients impose drastic conditions on doping techniques and thermal budget. To avoid these conditions, recently, junctionless MOSFETs have been proposed [1, 2]. The proposed devices would be fabricated without the need for forming junctions. Since the channel doping concentration and type are the same as in the source and drain extensions, there would be no doping concentration gradient, and therefore, no impurity diffusion during thermal processing steps. This should tremendously relax the thermal budget. The electrical characteristics of JLMOSFETs are identical to those of normal MOSFETs, however, the physics is quite different [3].

The main problems associated with MOSFET scaling are different effects which tend degrade device characteristics. Among the more important ones are: technological variability of parameters [4], short channel effects [5], influence of single defects in oxide or oxide-semiconductor interface [6]. The use of multiple-gate topologies significantly enhances the electrostatic integrity of the device and provides increased immunity from SCEs [7], however, in many simulation studies connected with short channel effects research do not take consider parasitic capacitance. In this work, the DIBL effect for trigate SOI Junctionless MOSFET with a gate length of 10 nm has been investigated in 3D simulation and the influence of parasitic capacitance connected with gate lateral extensions was considered.

In many practical cases for Integrated Circuits (MOSFET memory, CMOS based logic gates) a linear array of MOSFETs (Fig. 1), instead of single device, is used. In these cases all MOSFETs in a line can be covered by a common gate. This can lead to the extension L_{ext} of the lateral part of MOSFET's gate in the line compared to the gate of the single MOSFET (Fig. 2, a, b). The extended gate can alter the parasitic capacitances, and as a consequence, change the short channel effects in the nanometer MOSFET. For estimation of the influences of the extension of the gate lateral part on short channel effects, the DIBL effect in trigate SOI JLMOSFET with extended and unextended gates have been compared. For simulations, an Advanced TCAD Sentaurus device simulator has been used [8].

2. Results of simulation and discussion

A trigate SOI JLMOSFET with gate length $L_{gate} = 10$ nm and with silicon body width $W_{fin} = 10$ nm (Fig. 2) are simulated. We have considered transistors with an unextended gate as a simple contact (Fig. 2a) and with the extended polysilicon gate (Fig. 2b). The equivalent oxide thicknesses of the HfO_2 gate insulator used in simulation was 0.55 nm.

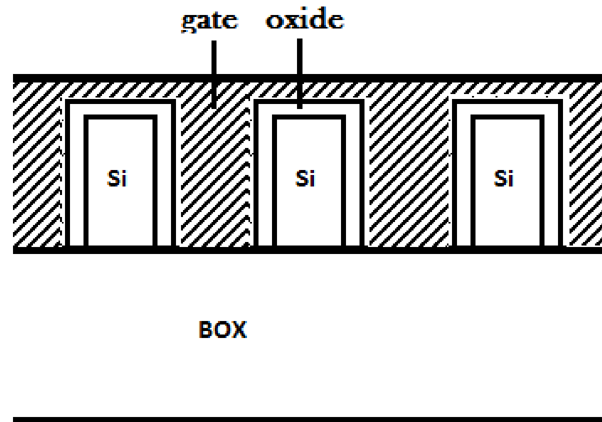

FIG. 1. SOI JLMOSFETs in the line

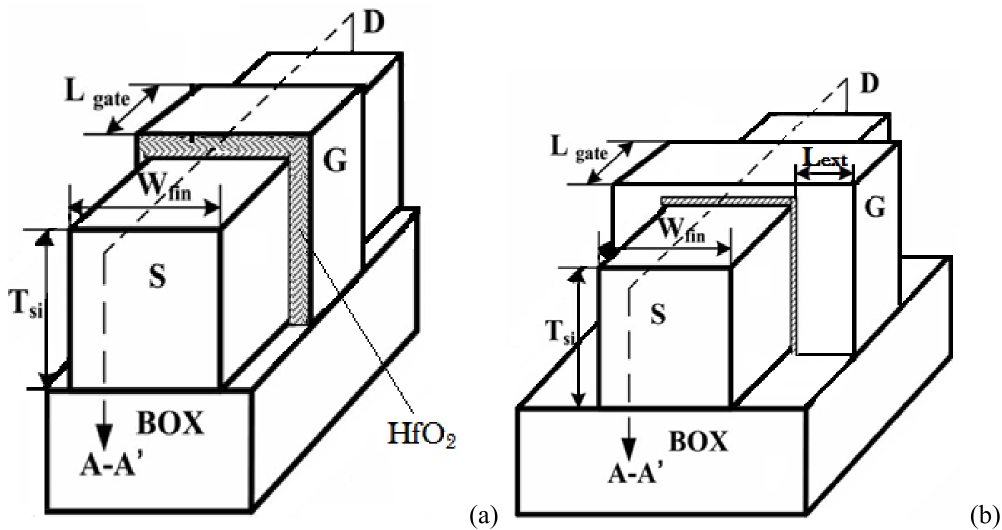

FIG. 2. Trigate SOI JLMOSFET with not extended (a) and extended (b) gate

For calculation of DIBL, we simulated transfer characteristics of JLMOSFETs with donor concentration in silicon layer $5 \cdot 10^{19}$ cm^{-3}, an active layer thickness $Tsi = 10$ nm. DIBL was calculated as change of threshold voltage per 1 V changing of drain voltage. The transfer characteristics were simulated for $Vds = 0.05$ V and 0.75 V. In Fig. 3 the transfer characteristics for the trigate JLMOSFETs with extended and unextended lateral gate part are shown. Id–Vg characteristics in Fig. 3 shows lateral extending of the gate leads to a change in the threshold voltage. DIBL effect are different for trigate SOI JLMOSFETs with extended and unextended gates. The value is higher in case of trigate JLMOSFETs with extended gate in all the considered range of L_{ext} (Fig. 4). It means that in the cases of trigate; for MOSFET with unextended gate, the threshold voltage was more controlled by the gate than by drain voltage. Such behavior for DIBL might cause additional change in the source (drain)-gate parasitic capacitance (Fig. 5) of the device structure.

In the considered case, an additional potential is induced in the source (drain) part of substrate by the lateral part of the gate through the parasitic source (drain)-gate capacitance coupling. It is expected that this influence is higher at high parasitic coupling capacitance. The parasitic source (drain)-gate capacitance can be considered as capacitance between two perpendicular bodies, i.e. the device's silicon body and gate (Fig. 5). This parasitic capacitance may be estimated using the non-parallel thick-plate capacitor approach [9]. According to this methodology, the parasitic capacitance is proportional to $\ln(1 + l/d)$, where l may be considered as a length of the gate extension L_{ext}, and d is some constant. As it can be seen from the expression, with increasing gate extension, the parasitic capacitance, as well as its influence on the source (drain) potential, is increased logarithmically and should reach saturation at higher gate extensions, L_{ext}. Such dependence is coordinated with the dependence of

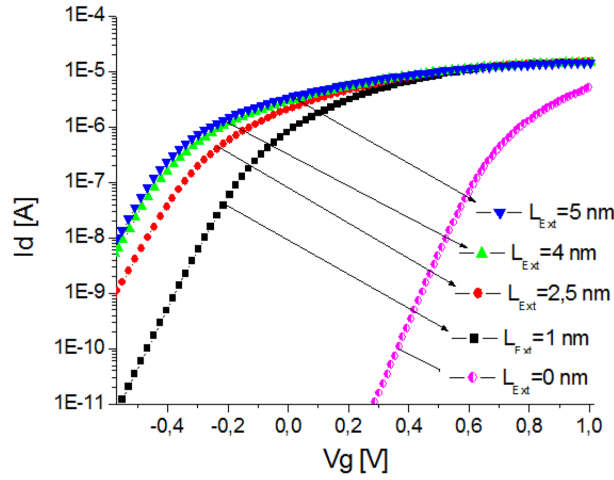

FIG. 3. Transfer characteristics for trigate JLMOSFETs with extended and not extended lateral part of gate, $Vds = 0.75$ V

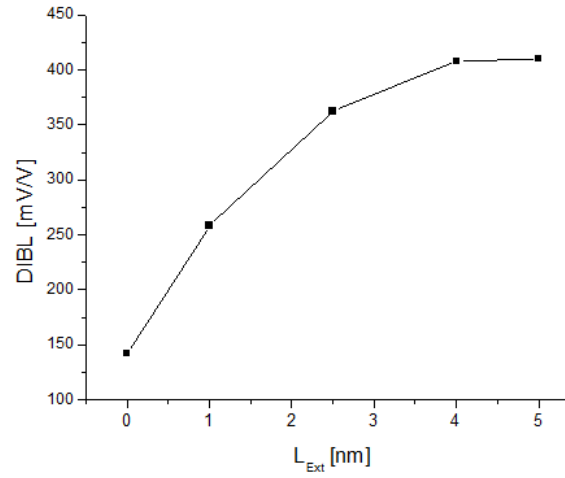

FIG. 4. DIBL dependence on length of lateral extension of the gate L_{ext}

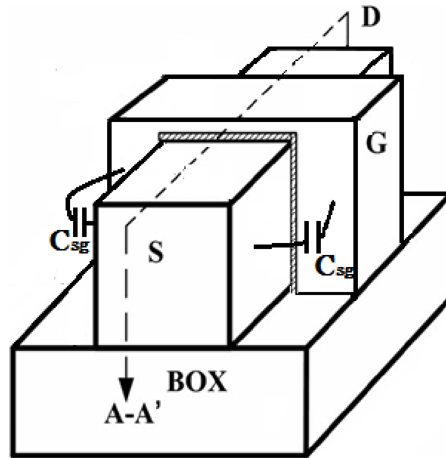

FIG. 5. Trigate JLMOSFET with the indicated source(drain)-gate parasitic capacitance Csg

DIBL on the gate lateral extension L_{ext}, which is shown in Fig. 4. In Fig. 6, potential distributions from source end to drain end along the center of silicon body for different L_{ext} at drain-source voltage $Vds = 50$ mV are shown. As it is seen from the figure the potential barrier between source and drain is lowered with increasing the lateral gate extension L_{ext}. In addition, the potential barrier between the source and drain also depends on drain-source voltage, too (see Fig. 7). In Fig. 7, the potential barrier was shown to change more for high L_{ext} with the same change of Vds. Such behavior of potential in the body results in DIBL dependence on the L_{ext} which is shown in Fig. 4.

3. Conclusion

Simulation of SOI JLMOSFET with a gate length of 10 nm, silicon body thicknesses and width of 10 nm shows that short channel effects such as DIBL for trigate devices with extended lateral gate portions are higher than those of the devices not having extended gates. The difference of DIBL for the devices with extended and unextended gates depends on lateral extension of gate L_{ext} and it occurs as a result of the influence of parasitic source (drain)-gate capacitance to the device body potential.

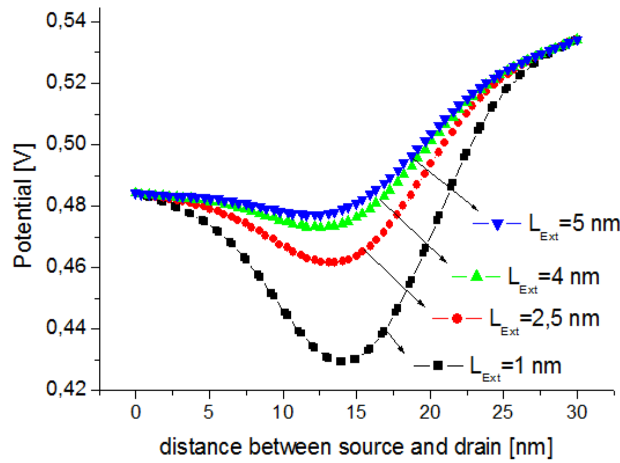

FIG. 6. Potential distribution along center of transistor's substrate from source end to drain end at different gate lateral extensions

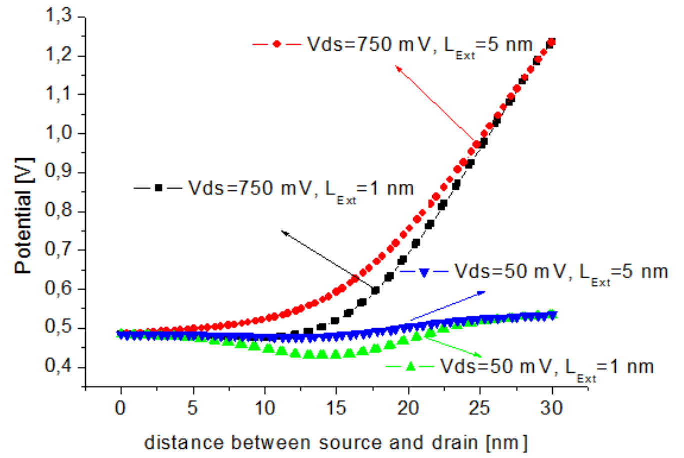

FIG. 7. Potential distribution along center of transistor's body from source end to drain end at gate lateral extensions 1 nm and 5 nm for $Vds = 50$ mV and $Vds = 750$ mV

References

[1] Park J.-T., Colinge J.-P., Diaz C.H. Pi-Gate SOI MOSFET. *IEEE Electron Device Letters*, 2001, **22** (8), P. 405–406.

[2] Lee C.-W., et al. Performance estimation of Junctionless multigate transistors. *Solid-State Electronics*, 2009, **54**, P. 97–103.

[3] Colinge J.-P. Conduction mechanisms in thin-film, accumulation-mode p-channel SOI MOSFETs. *IEEE Trans. Electron Devices*, 1990, **37**, P. 718.

[4] Abdikarimov A., Indalecio G., et al. Influence of device geometry on electrical characteristics of a 10.7 nm SOI-FinFET. *Proceeding of the 17th International Workshop on Computational Electronics (IWCE-17)*, Paris, France, 3–6 June 2014, P. 247–248.

[5] Veeraraghavan S., Fossum J.G. Short-channel effects in SOIMOSFETs. *IEEE Transactions on Electron Devices*, 1989, **36** (3), P. 522–528.

[6] Atamuratov A.E., Aminov U.A., et al. The lateral capacitance of nanometer MNOSFET with a single charge trapped in oxide layer or at SiO_2 – SI_3N_4 interface. *Nanosystems: Physics, Chemistry, Mathematics*, 2015, **6** (6), P. 837–842.

[7] Ferain I., Colinge C.A., Colinge J.-P. Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. *Nature*, 2011, **479**, P. 310–316.

[8] URL: http://www.synopsys.com.

[9] Bueno-Barrachina J.M., Cañas-Peñuelas C.S., Catalan-Izquierdo S. Capacitance Evaluation on Non-parallel Thick-Plate Capacitors by Means of Finite Element Analysis. *Journal of Energy and Power Engineering*, 2011, **5**, P. 373–378.