NANOSYSTEMS: PHYSICS, CHEMISTRY, MATHEMATICS, 2015, 6 (6), P. 837–842

The lateral capacitance of nanometer MNOSFET with a single charge trapped in oxide layer or at SiO_2 - SI_3N_4 interfaceat

A. E. Atamuratov[1], U. A. Aminov[2], Z. A. Atamuratova[2],
M. Halillaev[2], A. Abdikarimov[2], H. Matyakubov[2]

[1]Urganch Branch of Tashkent University of Information Technologies, Tashkent, Uzbekistan

[2]Urganch State Universityy, Tashkent, Uzbekistan

a.atamuratov@tuit.uz

PACS 85.30.Tv **DOI 10.17586/2220-8054-2015-6-6-837-842**

In this work the dependence between the position of single charge trapped in an oxide layer or at SiO_2 – Si_3N_4 interface and the concentration distribution of charge carriers on a semiconductor substrate surface of the nanometer n-channel Metal-Nitride-Oxide-Semiconductor Field Effect Transistor (MNOSFET) and p-channel MNOSFET with n^+ drain area is studied. It is shown that the lateral capacitances of nanometer MNOSFET depend on the position of single charge in oxide or at interface. This dependence allows one to estimate the position of trapped charges along the channel of transistor.

Keywords: Defects, lateral capacitances, oxide trapped charge, interface trapped charge, nanometer MNOSFET.

Received: 1 November 2015

1. Introduction

The ultra thin oxide layers of MOSFETs exhibit unusual behavior, such as atomic-scale heterogeneity in thickness and in composition. Even a small number of atomic-scale defects are problematic, as they can trap a superfluous amount of electrons or holes which can be sources for instability and degradation of MOSFET. Therefore, it is very important to investigate such defects. Macroscopic C-V methods show only the average properties of the area under gate without specification of exact spatial distribution of the trapped charge. In [1-6], by applying a technique of scanning tunnel microscopy, the spatial distribution of the trapped charge was shown. However these methods are labor-intensive, have limited speed of scanning and require the application of mechanical parts.

In this work, we study the dependence between the position of a single charge trapped in an oxide layer or on a SiO_2 – Si_3N_4 interface and the concentration distribution of charge carriers on a semiconductor substrate surface of MNOSFET. In particular, the source-substrate and drain-substrate transitions depletion layer width dependence on position is considered for a trapped single charge in an oxide layer and at interface. In the flat capacitor approximation, through the determination of depletion layer width, it is possible to estimate the capacity of the above-specified transitions and this can be used for obtaining information about the position of a trapped charge in an oxide layer or at the interface.

Prior works [5, 6] have stated that it is possible in SiO_2 to provide the density of states $3{\cdot}10^{13}$ cm^{-2}. For this density of states, one can calculate volume of space, where the single carrier can be located in an area with a linear size 1.8 nm. For simulation of single trapped charge influence on the carrier concentration distribution, the MNOSFET with an oxide layer

of thickness 1.8 nm was created. Captured single charge in an oxide layer is simulated by introducing the homogeneously distributed fixed charge with the surface density recalculated to the volume density. The length of the channel of considered transistor is 55 nm.

2. Simulation results and discussion

It is considered the width of depletion layer of a source-substrate transition with the single charge trapped in an oxide layer of nMNOSFET. For such a system, we calculated the depletion layer width d at various applied voltages and positions for the oxide layer-trapped charge. The source-substrate (drain-substrate) transition consists of two parallel parts: the source-channel and source-substrate parts. The trapped charge exerts its main influence on the source-channel part. Therefore, we consider the change of this part only. The depth of the channel from the Si-SiO_2 interface, where the changes of depletion layer width occur is appreciable, 10 nm. As an average, a depletion layer width of 5 nm depth from the surface of the substrate is considered. In Fig. 1, the charge carrier concentration distribution along the channel at various depths from surface of the semiconductor is shown for an applied voltage V=1. It can be seen that the width of transition at a depth 5 nm is equal to the total average.

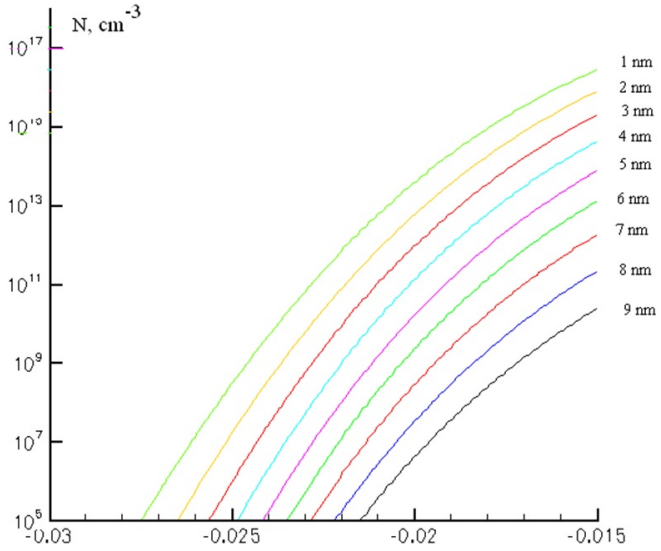

FIG. 1. Charge carrier concentration distribution along the channel at different depths from Si-SiO_2 interface

The transition capacitance can be found by the formula C $=\varepsilon\varepsilon_0$ S/d in the flat capacitor approximation. As the metallurgical border of lateral transitions do not change in charge trapping, the area of transition S also does not change. Therefore, the quantity C'=1/d is the main parameter which can be used for estimating the transition capacitance.

A negative voltage is applied to source substrate. In Fig. 2, the C' (V) dependence is shown for various positions of the trapped charge.

As it can be seen from this plot, the C'-V characteristics are non-monotonously displaced to area with high C' in all trapped charge positions. In Fig.3 the C', the dependence on position of oxide trapped charge at applied voltage 0V is shown. C' is increased when the trapped charge is positioned near the source end. At longer distances from the source end, C' monotonically decreases to a value corresponding to the case of absence of trapped charge.

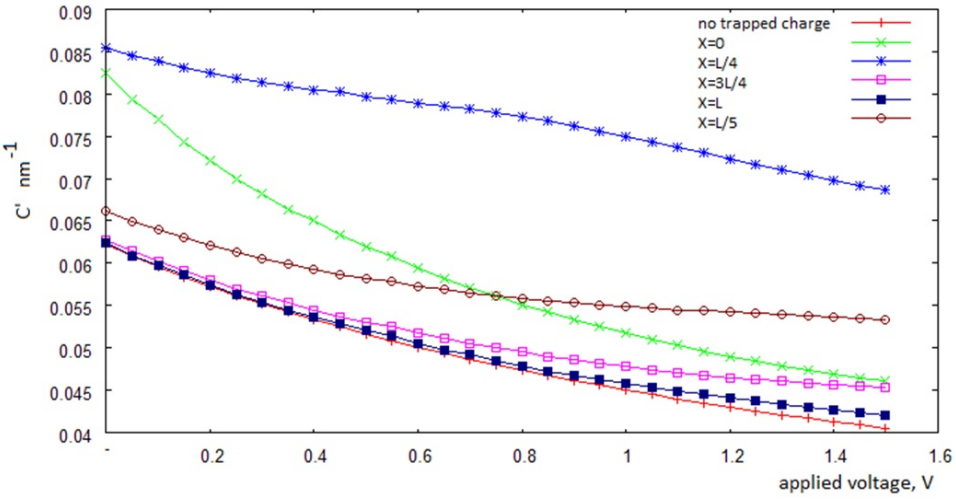

FIG. 2. C'(V) dependence for various positions of oxide trapped charge. X is the distance between center of the trapped charge and source end of oxide, L is the oxide length

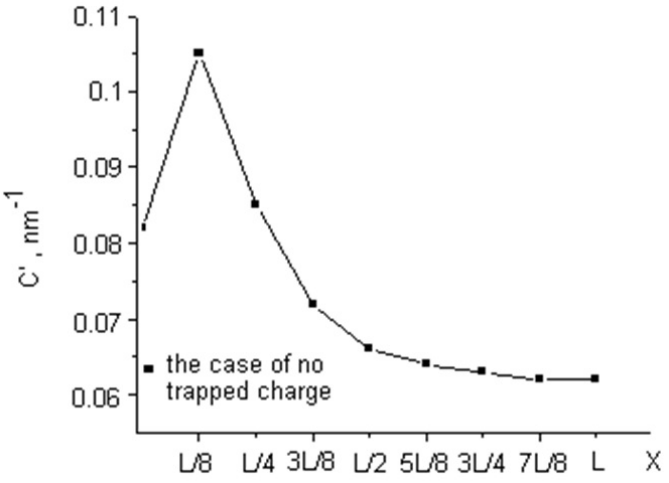

FIG. 3. C' dependence on position of oxide trapped charge at applied voltage 0V. X is the distance between the trapped charge center and source end of oxide, L is the oxide length

The charge trapped on a non-central area of oxide have different influences to the width of the depletion layer. One can obtain from this effect information about the position of the trapped charge. The dependences between the ratios of C' for source-substrate and drain-substrate transitions and position of the trapped charge is shown in Fig.4.

For ease of structure at lateral C-V measurement, it is reasonable to propose the p-channel MNOSFET with p^+ -source and n^+ -drain area. In case of such structure, one can consider the influence of single charge trapped at SiO_2 – Si_3N_4 interface to C(V) dependence (Fig.5). In this case, C'-V characteristics are also non-monotonically displaced to the area with high capacitance for all interface trapped charge positions (Fig. 6).

In order to study the possibility for detecting defect distribution by voltage scanning, we calculated derivative of C' over the voltage at different trapped charge positions. For

such the structure, the local minimum of dC'/dV can be observed for all trapped charge positions (Fig.7).

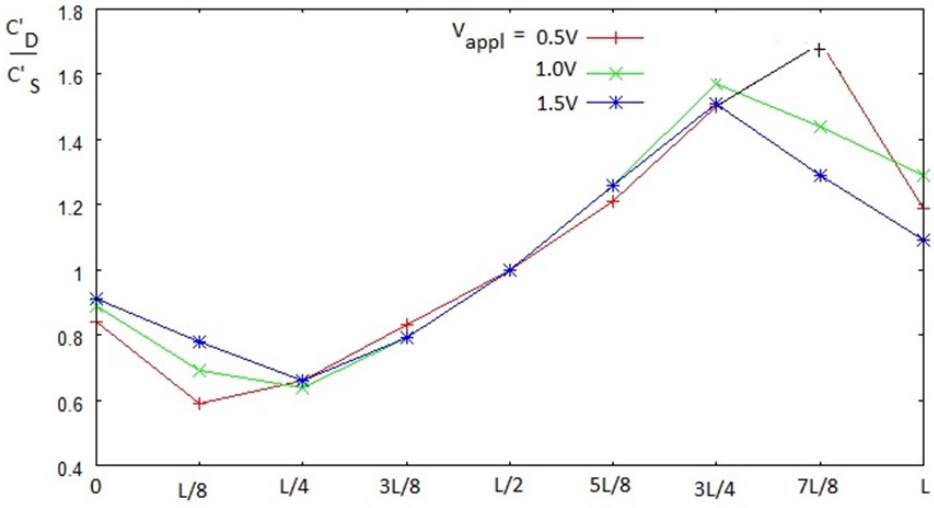

FIG. 4. Ratio of C' for source-substrate and drain-substrate transitions vs trapped charge position. C'_D is 1/d for drain-substrate transition and C'_S is 1/d for source-substrate transition. L is the length of oxide layer along channel

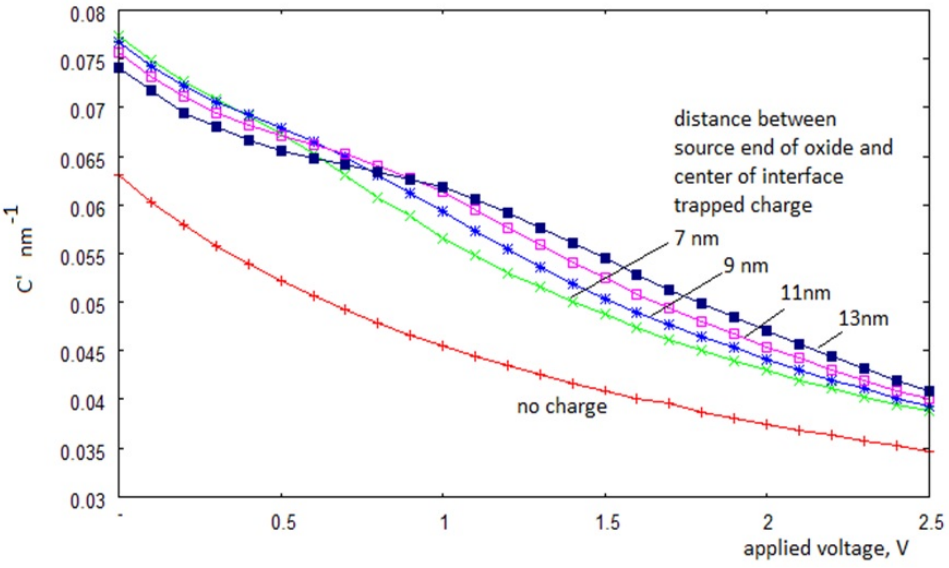

FIG. 5. C'(V) dependence for various positions of charge trapped on SiO_2–Si_3N_4 interface

The above results show that the values for the applied voltage corresponding to a local minimum of dC'/dV depend on the position of the trapped charge. This value increases with removal of the trapped charge from source edge (Fig 8). This dependence has a monotonic character and allows one to identify the positions of defects along the channel of MNOSFET.

3. Conclusion

The nanometer n-channel MNOSFET with n^+ -source and drain area and p-channel MNOSFET with p^+ -source and n^+ - drain area is studied in this work. For the n-channel

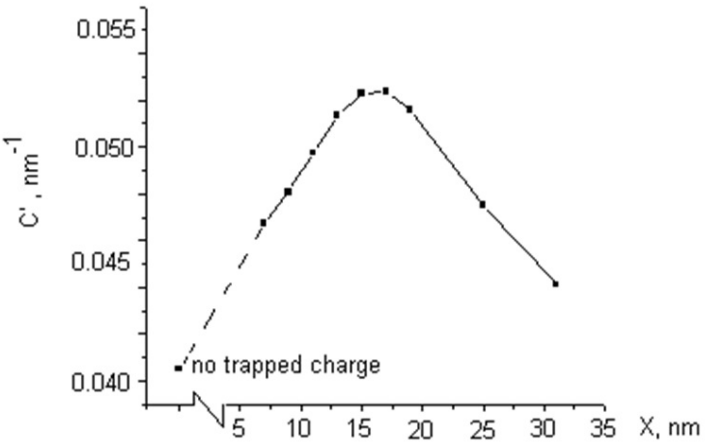

FIG. 6. C' dependence on positions of charge trapped on SiO_2–Si_3N_4 interface. X is the distance between source edge and center of trapped charge area. Applied source-substrate voltage is 1.5 V

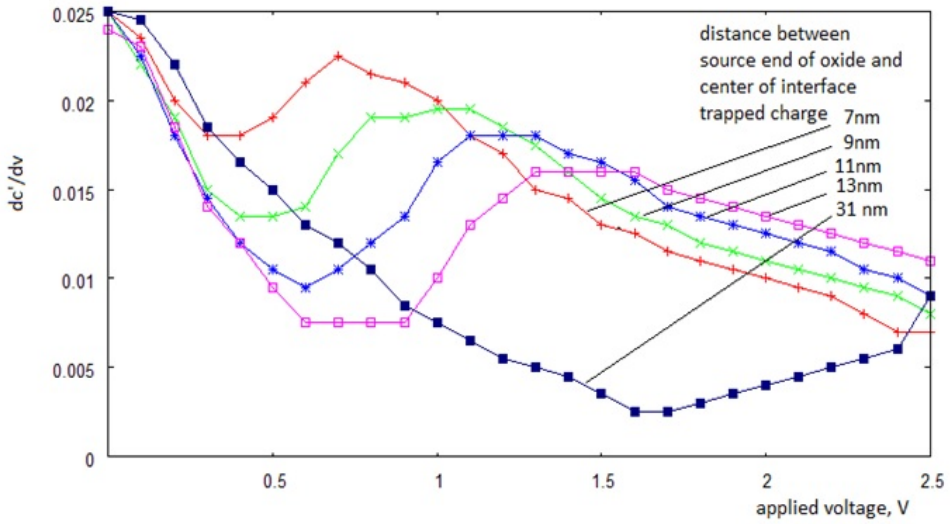

FIG. 7. dC '/dV vs source-drain voltage for different position of interface trapped charge

MNOSFET, C' increases when the position of trapped charge is close to the source and decreases at longer distances from the source. The dependence of the C'_d /C's ratio on the position of the trapped charge shows that positioning of the trapped charge on left half of oxide makes this ratio less than 1. Accordingly, localization on right (drain) half of the oxide makes this ratio greater than 1. Such relations allow one to estimate the positions of the charged defects relative to the center of channel.

For p-channel MNOSFET with n^+ - drain area, positioning of a trapped charge near the source edge of SiO_2-Si_3N_4 interface increases C'. With increased distance from the source edge, at a certain distance, C' monotonically decreases. Local minima in the dC'/dV dependence on voltage were also observed. The bias voltage values corresponding to these minima depend on the position of the trapped charge along the channel. Such dependence allows one to define the distribution of charge defects at the interface along the channel.

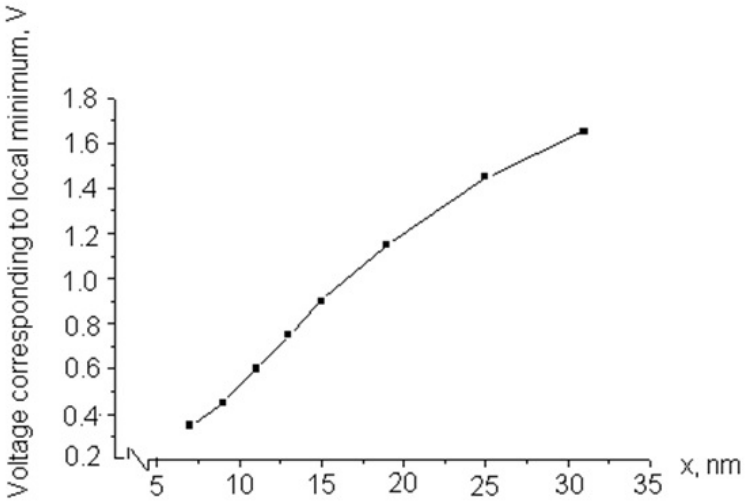

FIG. 8. Dependence between value of applied voltage corresponding to local minimum of dC'/dV and position of trapped charge along channel

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