

SUPPLEMENTARY MATERIALS for How to make opposite state store again

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Supplementary materials

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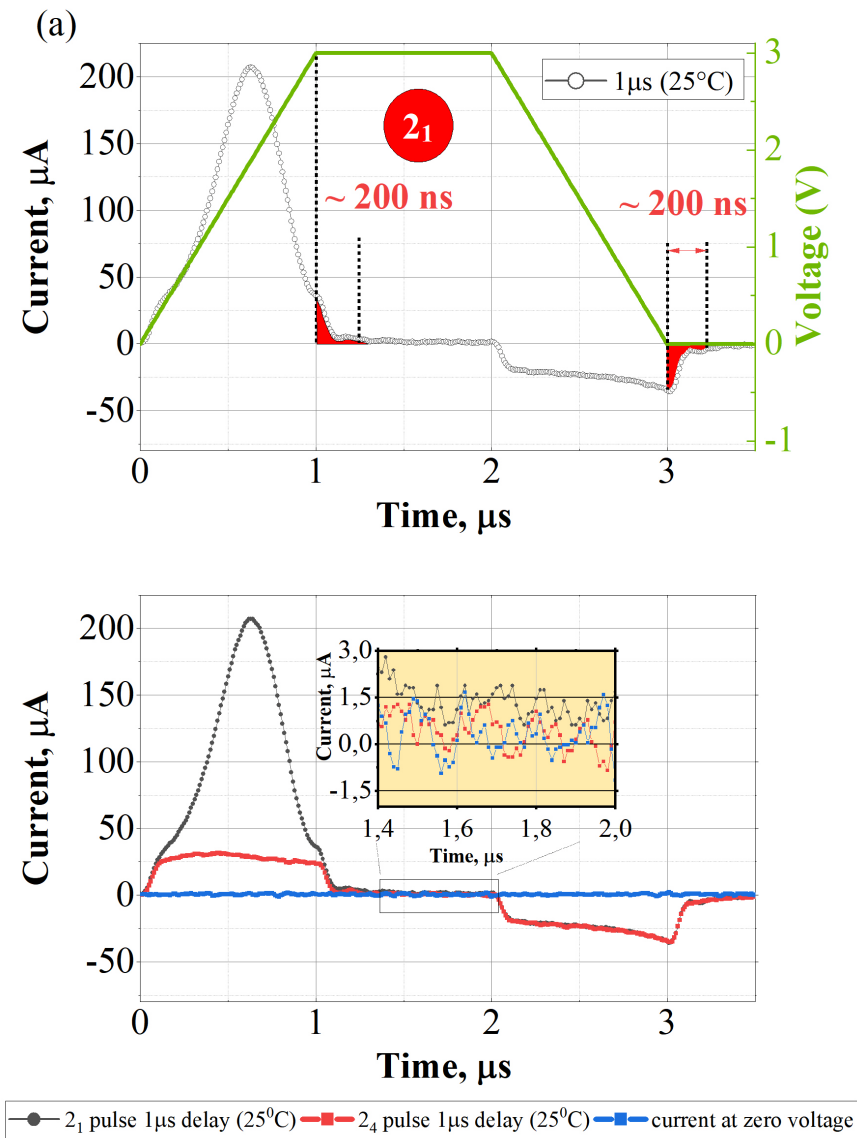


FIG. S1. RC delay at voltage pulse (a) and current responses (b) of pulses from 21 (black), 24 (red) and without applied voltage (blue) before baking where inset demonstrate current level at pulse shelf

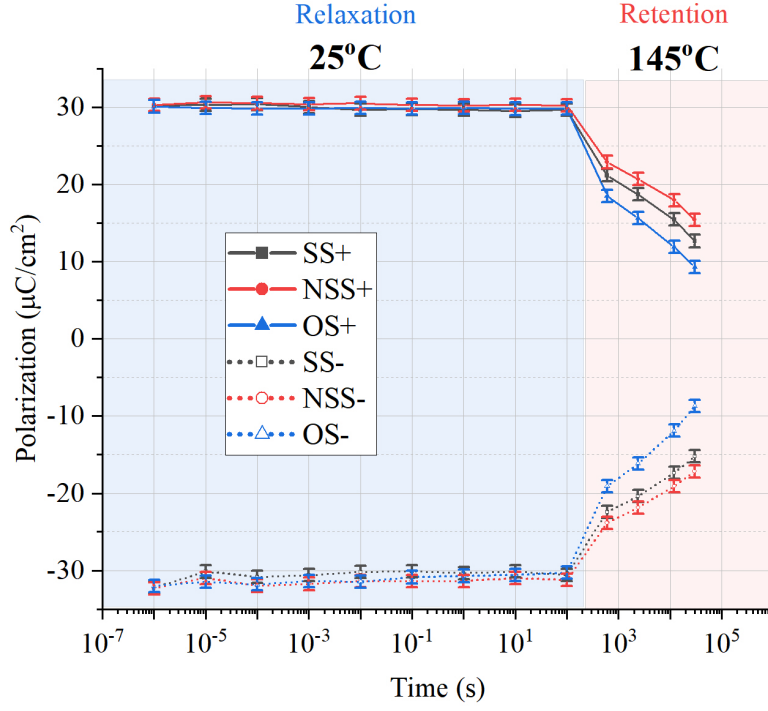


FIG. S2. Relaxation (blue area) and Retention (red area) measurements of the TiN/HZO/TiN capacitors for SS+, NSS+, OS+ and SS-, NSS-, OS-. Charge measurement range was $3.5 \mu\text{s}$ (pulse width and 500 ns after it)

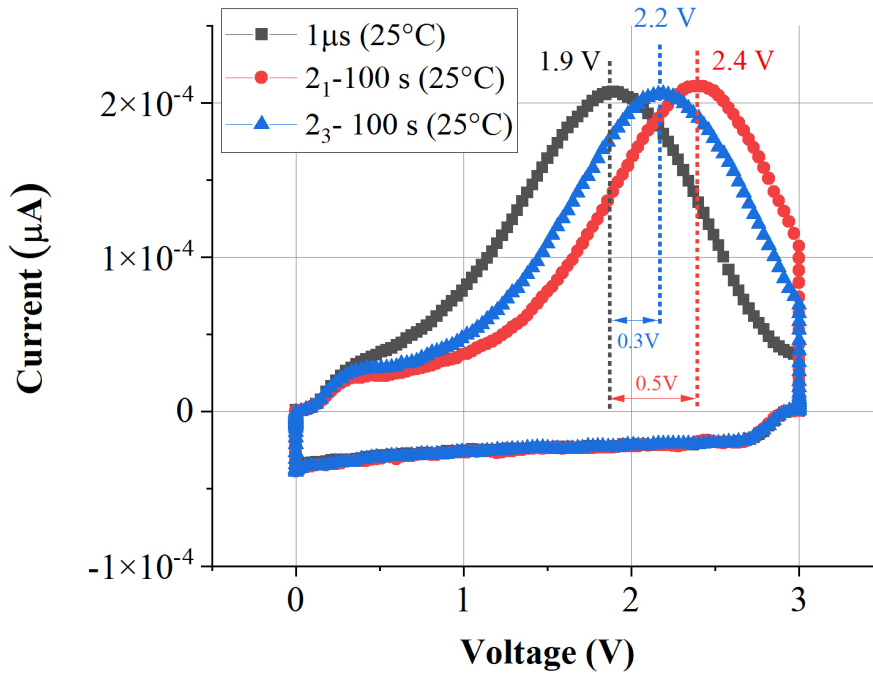


FIG. S3. The effect of an imprint in the relaxation time interval. The black curve is identical for pulses 2_1 and 2_3 with a delay of 1 microsecond, red curve for 2_1 pulse with a delay of 100 second, blue curve for 2_3 pulse with a delay of 100 second

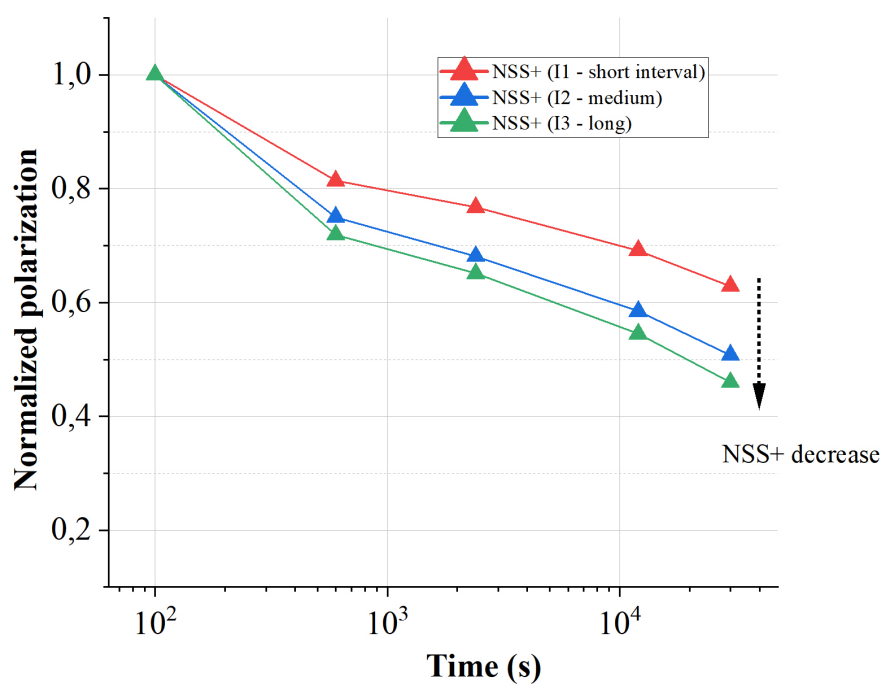


FIG. S4. Comparison of normalized polarization loss of NSS+ for different integration intervals after baking at 145 °C